

A ripple-mitigating pre-amplifier based on interleaved DC-DC boost converters for efficiency improvement

Pre-Amplificador de potencia basado en conexión paralela de convertidores DC-DC para reducción de rizados de corriente e incremento de eficiencia

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(Recibido el 9 de diciembre de 2010. Aceptado el 20 de junio de 2011)

Abstract

An efficient pre-amplifier based on interleaved DC-DC boost switching converters to mitigate high-frequency harmonics injection to power sources is proposed. The main features of the pre-amplifier are mitigate the ripple of power converters input-current and improving the efficiency of the whole power conversion chain. The pre-amplifier optimal operating conditions are calculated, and the circuit is modeled and controlled to operate in such conditions. The pre-amplifier interacting with a classical single boost is analyzed, obtaining a strong reduction in the current ripple injected to the source, and also improving the efficiency of the initial conversion system. Finally, the theoretical analyses are confirmed by means of circuital PSIM simulations and experimental results.

----- *Keywords:* Pre-Amplifier, interleaved converters, efficiency improvement, ripple mitigation

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Resumen

Este artículo propone un pre-amplificador basado en convertidores DC-DC conectados en paralelo para la reducción de armónicos inyectados a fuentes de potencia. Las principales características del pre-amplificador son la reducción del rizado de corriente de entrada en convertidores de potencia, incrementado además la eficiencia del sistema de conversión. Se describe el cálculo de las condiciones óptimas de operación del pre-amplificador, así como su modelado matemático y control para operar en las condiciones seleccionadas. Así mismo, se analiza el pre-amplificador con un convertidor elevador clásico, obteniendo una reducción significativa en el rizado de corriente inyectado a la fuente, así como un incremento en la eficiencia del sistema. Finalmente, los análisis teóricos se confirman a través de simulaciones circuitales y resultados experimentales.

----- *Palabras clave:* Pre-Amplificador, conexión en paralelo, eficiencia, reducción de rizado

Introduction

Considering the problematic that establishes the global warming, fossil fuel exhaustion and the need to reduce carbon dioxide emissions provided the stimulus to develop renewable energies sources as fuel cell and photovoltaic panels [1, 2]. These options have been outlined for being two of the most attractive since they are clean, pollution free, and inexhaustible. An important aspect to consider is that these options have a series of disadvantages as the high costs of installation and maintenance, low diffusion among the users and difficulties in the process of energy storage, and such characteristics maintain them non-competitive opposite to the option of fossil-based energy resources. The appearance of new types of semiconductors, control strategies and switched devices has raised the relation cost benefit for this type of applications [3-6]. Nevertheless, the interconnection with the utility grid continues to be a weak point to consider.

It is widely known that the current harmonics generated in source-power converter interaction can seriously affect the system integrity and performance. In fuel cell applications, the current harmonics are directly related to the Oxygen-starvation phenomena, which considerably increase the natural aging of the cell membranes

[7]. As for the photovoltaic applications, the current harmonics affect the performance of the control strategy, like the Maximum Power Point Tracking (MPPT) controller, reducing its accuracy and decreasing the system efficiency [8]. In this paper, the current harmonic injection to power sources by power converters is addressed through an active cancelation. Nevertheless, low frequency oscillations at double of the grid frequency are not considered since they can be addressed by control approaches [9].

This paper is based on the work “A Ripple-Mitigating Pre-filter Based on Interleaved DC-DC Boost Converters”, developed by the authors, which appeared in the 36th Annual Conference of the IEEE Industrial Electronics Society (IECON-2010, © 2010 IEEE), and it is focused on the development of a power conversion system able to mitigate the high frequency current harmonics generated during the converter switching, which is traditionally addressed by the typical capacitor-filtering solution [10]. The proposed solution also reduces the input capacitor requirements, decreasing its cost and avoiding the use of non-reliable electrolytic capacitors.

The remain of the paper is organized as follows. The next section analyses a classical single boost converter considering power losses. Then,

the novel pre-amplifier structure considering two boost converters in interleaved topology is introduced. Furthermore, the paper presents the proposed pre-amplifier operating with a boost converter, and compares it with the classical boost approach by analytical and PSIM simulation results. Moreover, the proposed solution is validated by means of experimental results. Finally, some conclusions of the work are given.

Single boost converter analysis

The design of a DC-DC converter, boost in this case, is performed to obtain the desired current and voltage ripples. Given the switching frequency, the input and output voltage, and ripples allowed, the capacitance and inductance are designed, which are largely responsible for the converter's size. The first step is to analyze the DC-DC boost converter efficiency considering the power losses lumped in a single inductor series-resistance as depicted in figure 1. Using the volt-second balance [11] (1), the relation between the input and output voltages (2) is obtained, where T is the switching period and D the steady-state duty cycle.

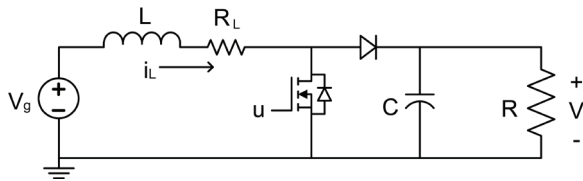


Figure 1 Boost converter topology considering parasitic losses

$$\langle V_L \rangle = \frac{1}{T} \int_0^T V_L dt = 0 \quad (1)$$

$$\frac{V}{V_g} = M(D) = \frac{1}{(1-D)} \left(1 + \frac{R_L}{(1-D)^2 R} \right) \quad (2)$$

Considering the capacitor charge balance [11] (3), the steady state inductance's current i_L is:

$$\langle I_C \rangle = \frac{1}{T} \int_0^T I_C dt = 0 \quad (3)$$

$$I_L = \frac{V_g}{R(1-D)^2 + R_L} \quad (4)$$

The current ripple in the inductor is obtained calculating the current's slope in the first switching semi-cycle (5). Similarly, the voltage ripple at the output capacitor (6) is calculated.

$$\Delta I_L = \frac{V_g DT}{2L} \left(1 - \frac{R_L}{R(1-D)^2 + R_L} \right) \quad (5)$$

$$\Delta V = \frac{VDT}{2RC} = \frac{V_g}{2RC(1-D)} \left(\frac{1}{1 + \frac{R_L}{(1-D)^2 R}} \right) \quad (6)$$

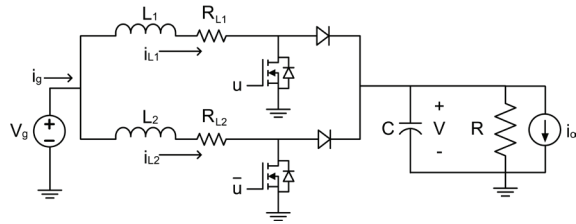
Finally, the efficiency of the boost converter considering the parasitic losses is given by (7).

$$\eta_F = \frac{1}{1 + \left(\frac{R_L}{(1-D)^2 R} \right)} \quad (7)$$

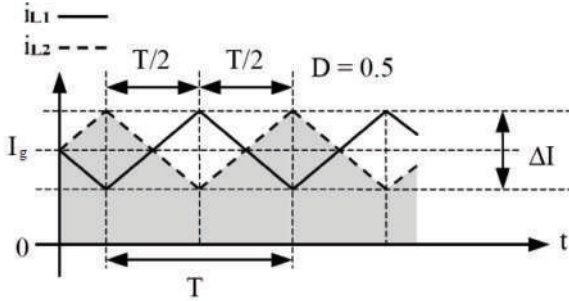
Pre-Amplifier topology and control

The pre-amplifier consists of two boost converters in parallel, analyzed by considering the power losses lumped in inductor series-resistances, which scheme is depicted in figure 2(a). The active switches, MOSFETs in this case, are controlled using complementary signals. This structure is called complementary interleaving and allows reducing the ripple of the input and output variables according to the specifications. The complementary activation of the switches in the boost converters cancels inductors current harmonics reducing the ripple in the input current [1].

Also, it mitigates the output voltage ripple and reduces the electromagnetic interferences. In this way, the reduction of the ripples allows to reduce the converter capacitances.



(a) Electrical scheme



(b) Inductor current waveforms

Figure 2 Pre-amplifier considering losses

With the complementary control signals, one of the inductors current is increasing while the another one current is decreasing, therefore, the slopes of the current waveforms have opposite signs as depicted in figure 2(b), where T represents the switching period, D the duty cycle and ΔI the peak-to-peak ripple current. Since the input current is the sum of both inductor currents, the resulting slope tends to zero producing a decrease in the input current ripple. As shows figure 2(b), the most favorable ripple decreasing case is produced when the duty cycle is 0.5, or 50 %, because the slopes of both currents are equal but with opposite sign. The final value of the input current I_g corresponds to the integral of the shaded area.

Dynamic model

The state equations of the pre-amplifier circuit given in figure 2(a) can be expressed as:

$$\dot{X} = AX + BY \quad (8)$$

where X and \dot{X} correspond to the state variables vector and its derivatives. The Y vector contains

the system inputs, and A and B matrices depend on the converter parameters.

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v \end{bmatrix}, \quad \dot{X} = \begin{bmatrix} \frac{\partial i_{L1}}{\partial t} \\ \frac{\partial i_{L2}}{\partial t} \\ \frac{\partial v}{\partial t} \end{bmatrix}, \quad Y = \begin{bmatrix} V_g \\ i_o \end{bmatrix} \quad (9)$$

As is described in (9), the system states are the inductor currents i_{L1} and i_{L2} , and the output capacitor voltage v . The inputs of the system are the input voltage V_g , and the load perturbation current i_o . In steady state, the derivatives of states are zero, and the vector X is obtained as:

$$X = -A^{-1}BY \quad (10)$$

$$X = \frac{V_g}{R_{L1}R_{L2} + R(R_{L1}D^2 + R_{L2}D'^2)} \begin{bmatrix} R_{L2} + RD(D-D') \\ R_{L1} + RD'(D'-D) \\ R(R_{L1}D + R_{L2}D') \end{bmatrix} \quad (11)$$

In sake of simplicity, the losses of both converters are considered similar, $R_L \approx R_{L1} \approx R_{L2}$, and expression (11) can be simplified as:

$$X = \frac{V_g}{R_L + R(D^2 + D'^2)} \begin{bmatrix} 1 + \frac{R}{R_L} D(D-D') \\ 1 + \frac{R}{R_L} D'(D'-D) \\ R \end{bmatrix} \quad (12)$$

The relation between the input and output voltages, obtained from the volt-second balance, is:

$$\frac{V}{V_g} = M(D) = \frac{1}{(R_L/R) + 2D^2 - 2D + 1} \quad (13)$$

Such a condition is valid for a duty cycle equal to 50 %, or $D = 0.5$. Otherwise, the pre-amplifier enters in Discontinuous Conduction Mode

(DCM) preventing the cancelation of the current ripples. This conclusion is obtained by applying the volt-second balance in each inductor:

$$L_1 : V_g D + (V_g - V) D' = 0 \Rightarrow D' = \frac{V_g}{V} \quad (14)$$

$$L_2 : (V_g - V) D + V_g (D') = 0 \Rightarrow D = \frac{V_g}{V} \quad (15)$$

From equations (14) and (15) is concluded that the only condition that ensures a Continuous Conduction Mode (CCM) for the pre-amplifier is given by:

$$D = D' = 0.5 \quad (16)$$

Simulations depicted in figure 3 corroborate the previous conclusion, where the inductor drove by the smallest duty cycle operates in DCM, and therefore the duty cycles of both converters must be $D = 0.5$ to operate in CCM and to obtain the desired current ripple reduction. Also, from equation (13), and considering a common relation between parasitic loss-resistance and load equal to 1%, the voltage conversion ratio of this pre-amplifier is approximately 2.

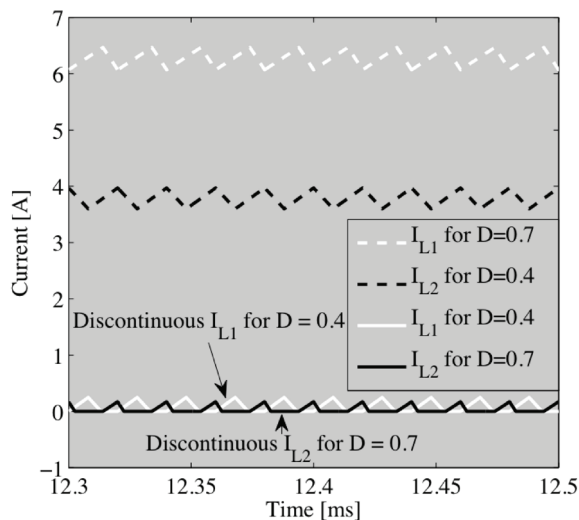


Figure 3 Simulation of inductor currents for $D \neq 0.5$. The current ripple magnitudes on the inductors are given by equations (17) and (18), obtained

solving the charge balance (3) for each inductor in steady-state conditions:

$$\Delta i_{L1} = \frac{V_g}{L} DT \quad (17)$$

$$\Delta i_{L2} = \frac{V_g}{L} (1 - D) T \quad (18)$$

Considering $D = 0.5$, the current ripple magnitudes (17) and (18) are equal but with opposite sign. This implies that the input current will have a small ripple, and in the ideal case, null ripple.

For $D \neq 0.5$ one inductor enters on DCM because the CCM conditions given by (14) and (16) are not fulfilled. The inductor drove by the smaller duty cycle, and therefore with lower steady-state current, enters on DCM. This is illustrated in figure 3, where a duty cycle $D = 0.7$ causes a discontinuous L_2 current since it is driven by D' , while $D = 0.4$ causes a discontinuous L_1 current.

The output voltage ripple, depicted in figure 4, is calculated by analyzing the current waveforms of the load $i_o(t)$ and output capacitor $i_c(t)$. Figure 4 shows that the output voltage ripple is small enough to consider the load current to be constant and equal to its steady-state value. The current ripple is a sawtooth waveform with a frequency equal to the double of the switching frequency.

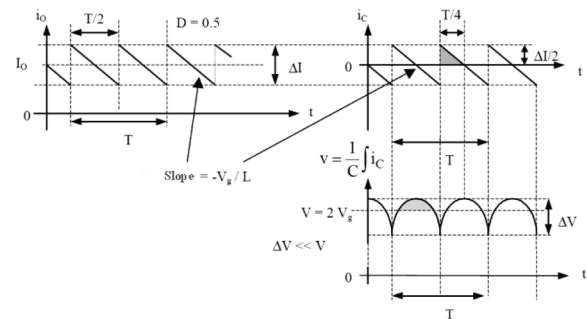


Figure 4 Load and output capacitor current waveforms

The voltage ripple is obtained by integrating the current ripple on the capacitor in each semi-period. It is observed in figure 4 that in each $T/4$

seconds the capacitor current sign changes, hence the capacitor voltage waveform is a symmetric convex parabola with a maximum value of $(2V_g + \Delta V/3)$. Calculating the integral of $i_c(t)$ through the triangular shaded area, the amplitude in absolute value of the output voltage ripple ΔV is calculated as:

$$\Delta V = \frac{T^2}{32LC} V_g \quad (19)$$

From the inductors current ripple cancelation is expected a null input current ripple, but since in each switching interval the output port and the input source are connected through one inductor, L_2 during DT seconds and L_1 during $D'T$ seconds, an input current ripple is generated by the output voltage ripple following the small-signal relation [12]:

$$L \frac{di_g}{dt} + R_L i_g = -v \quad (20)$$

Since the current ripple frequency in the output capacitor should be high, its losses are small enough to be neglected. Therefore, integrating the shaded area in capacitor voltage waveform of figure 4 and dividing it by L , the amplitude of the input current ripple ΔI_g is obtained as follows:

$$\Delta I_g = \frac{T}{9\sqrt{3}L} \Delta V \quad (21)$$

Sliding-mode control

In practical implementations, there is slightly different impedances in both pre-amplifier branches, which causes a difference between the DC current components of the inductors depending on its inductance and parasitic losses tolerances. This must be addressed to ensure the ripple reduction, and therefore a closed loop control system is required. Since the PWM technique requires an external periodic signal, the sliding-mode technique has been adopted due to its simpler implementation.

The first step in sliding-mode control consists in the design of the state space region to which the dynamic of the system must be restricted, being generally called sliding surfaces. One option is to choose hyperplanes [2], meaning linear combinations of the system state variables.

There are three state variables in the pre-amplifier. Two are the inductor currents and the last one is the voltage of the output capacitor. Although there are two switches, they are considered as a single control variable because they are activated by complementary signals, and therefore a single sliding surface $S(x)$ is required to fulfill the desired condition $D = 0.5$:

$$S(x) = i_{L1} - i_{L2} = 0 \quad (22)$$

The small-signal dynamics are defined by:

$$x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v \end{bmatrix}, u = \begin{bmatrix} V_g \\ i_o \end{bmatrix}, \dot{x} = Ax + \delta + u(Bx + \gamma) \quad (23)$$

From the sliding-mode control theory [4] and the system description, matrices A , δ , B and γ are:

$$A = \begin{bmatrix} \frac{-R_{L1}}{L} & 0 & \frac{-1}{L} \\ 0 & \frac{-R_{L2}}{L} & 0 \\ \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix}, \delta = \begin{bmatrix} \frac{V_g}{L} \\ \frac{V_g}{L} \\ \frac{-i_L}{C} \end{bmatrix} \quad (24)$$

$$B = \begin{bmatrix} 0 & 0 & \frac{-1}{L} \\ 0 & 0 & \frac{-1}{L} \\ \frac{-1}{C} & \frac{1}{C} & 0 \end{bmatrix}, \gamma = \theta \rightarrow \text{null matrix} \quad (25)$$

where the input voltage V_g is considered constant and positive, and the inductances are equal.

The equivalent control technique [2, 5] is used to calculate the continuous value u_{eq} to be taken by the control variable (22) if the conditions $S(x) = 0$ and $dS(x) / dt = 0$ are achieved. Such conditions guarantee that the system trajectory is tangent to $S(x)$ and remain trapped into it. The expression for the equivalent control is described by equation (26). In the numerator of the equivalent control there is the vector field $(Ax + \delta)$ whose expression, in this case, is given by equation (27), and likewise the denominator vector field is described by (28).

$$u_{eq} = -\frac{\{\nabla S, (Ax + \delta)\}}{\{\nabla S, (Bx + \gamma)\}} \quad (26)$$

$$Ax + \delta =$$

$$\left[\frac{V_g - v - R_{L1}i_{L1}}{L} \quad \frac{V_g - R_{L2}i_{L2}}{L} \quad \frac{i_{L1} - i_{L2}}{L} - \frac{v}{RC} \right]^T \quad (27)$$

$$Bx + \gamma = \left[\frac{v}{L} \quad \frac{-v}{L} \quad \frac{i_{L2} - i_{L1}}{C} \right]^T \quad (28)$$

The equivalent control expression depends on the parasitic losses and state variables, and also on the system inputs V_g and i_o . In sake of simplicity, the inductors parasitic losses are considered comparable, therefore $R_{L1} \approx R_{L2} \approx R_L$, and the equivalent control is simplified to:

$$u_{eq} = \frac{R_L(i_{L1} - i_{L2})}{2v} + \frac{1}{2} = \frac{R_L S(x)}{2v} + \frac{1}{2} \quad (29)$$

Taking into account the transversality condition ($v \neq 0$), if the system trajectory is on the surface $\{S(x) = 0, i_{L1} = i_{L2}\}$, the equivalent control is constant and equal to 0.5 (30), while the switching frequency depends on the operating conditions.

$$u_{eq} = 0.5 \quad (30)$$

The controller has been implemented using the structure described in figure 5, where u and \bar{u} are the complementary signals for activating

the MOSFETs, and Δi_{LS} defines the maximum difference allowed between the inductor currents, therefore the width of the sliding surface.

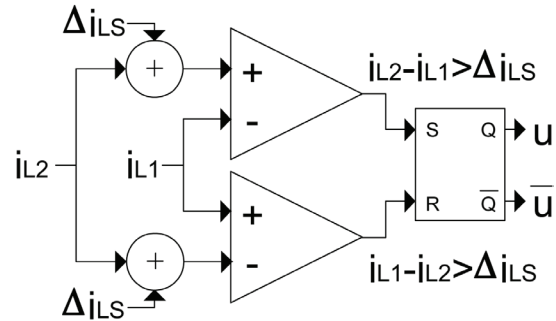


Figure 5 Control structure of the pre-amplifier

To illustrate the controller behavior, figure 6 shows a transient simulation where also in such conditions the inductor currents are complementary and the input current is minimum. In the simulation the input current is shown divided by two to allow its visualization in the same scale.

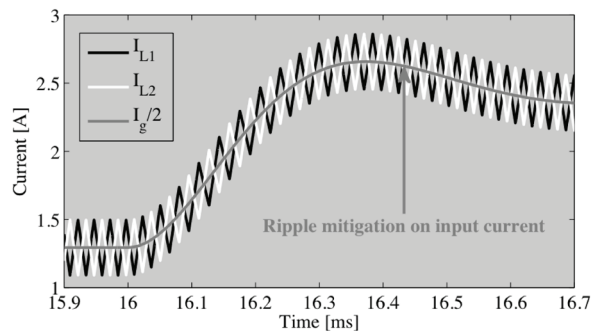


Figure 6 Dynamic simulation of inductor currents and input current for the pre-amplifier

Pre-Amplifier based system: classical boost interaction

This section analyses the proposed Pre-Amplifier interacting with a classical boost converter as depicted in figure 7. The main objective of this structure is to reduce the current ripple injected to the source V_g without reducing the original power conversion efficiency. In this section, the input current ripple and the efficiency of both boost and boost with active pre-amplifier are contrasted.

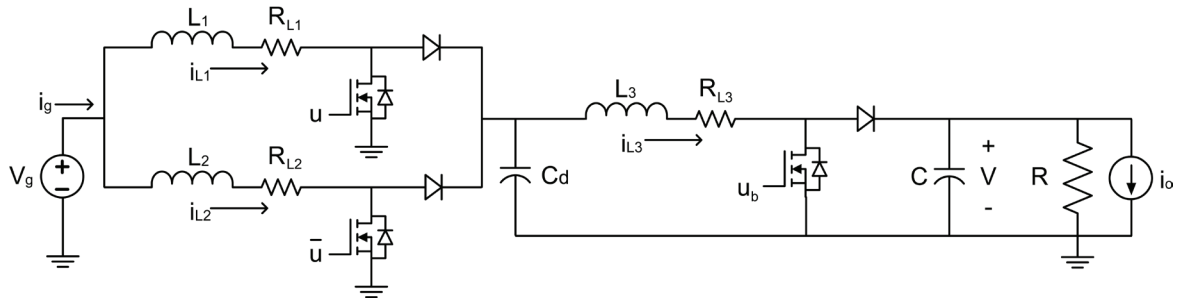


Figure 7 Pre-Amplifier interacting with a classical boost converter

Steady-state analysis of the pre-amplifier based system

By applying the volt-second balance, and considering $R_{L1} \approx R_{L2} \approx R_L$, the input-to-output voltage conversion ratio is:

$$\frac{V}{V_g} = M(D) = \frac{2(1-D)R}{(1-D)^2 R + R_{L3} + 2R_L} \quad (31)$$

Similarly, by applying the charge balance on the circuit, the steady-state input current is:

$$I_g = \frac{2V}{(1-D)(R + 2R_L)} \quad (32)$$

Finally, the efficiency of the complete conversion system is:

$$\eta_F = \frac{1}{1 + \left(\frac{R_{L3}}{(1-D)^2 R} \right) + \left(\frac{2R_L}{(1-D)^2 R} \right)} \quad (33)$$

Comparison between pre-amplifier based solution and classical single boost

To perform a fair comparison, the power converters must be analyzed in the same conversion ratio condition and under the same load and source characteristics. The pre-amplifier based system has a higher voltage conversion ratio $M(D)$ than the typical boost under the same source and load characteristics for a given duty cycle D . This is observed in figure 8, where considering a losses

ratio $R_L/R = 0.005$, or 0.5 %, a $M(D) = 6$ is obtained by operating the boost converter in the pre-amplifier based system at $D = 0.72$, while in single boost solution $D = 0.88$ is required. This is important since in boost converters the efficiency decrease with increments in D [11].

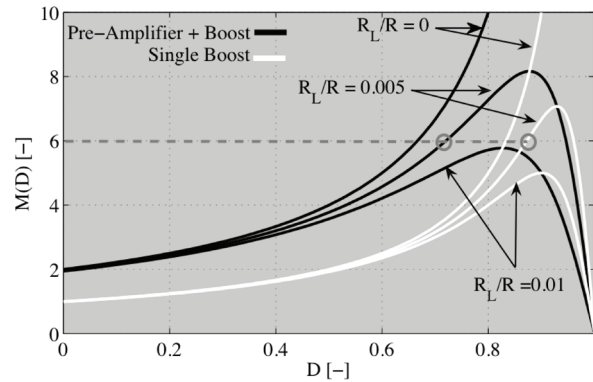


Figure 8 Voltage conversion ratio of both pre-amplifier based and single boost solutions

The pre-amplifier based system generates currents in each of the three inductors equal to the half of the inductor current in the single boost solution. Since the power losses depend on the square of the current, the losses in the pre-amplifier based solution are lower. This is depicted in figure 9, where considering $M(D) = 6$ and $R_L/R=0.005$, the pre-amplifier based solution provides an efficiency of 0.83, or 83 %, while the single boost provides an efficiency of 0.76, or 76 %. Considering a different R_L/R condition, the pre-amplifier solution also provides higher efficiency.

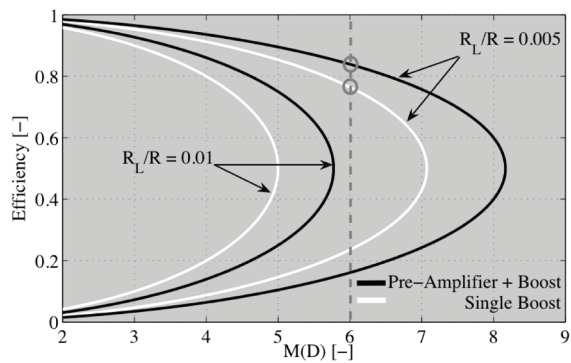
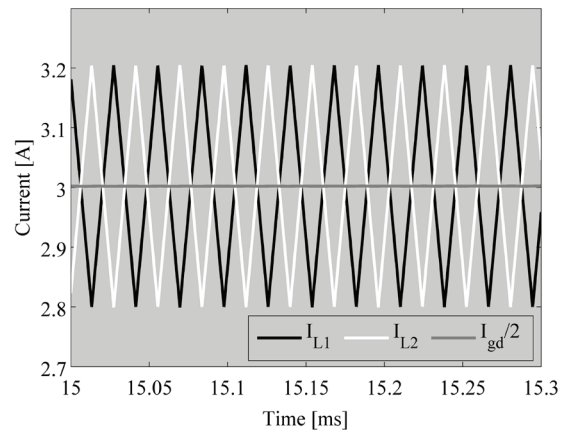


Figure 9 Efficiency vs. conversion ratio of both pre-amplifier based and single boost solutions

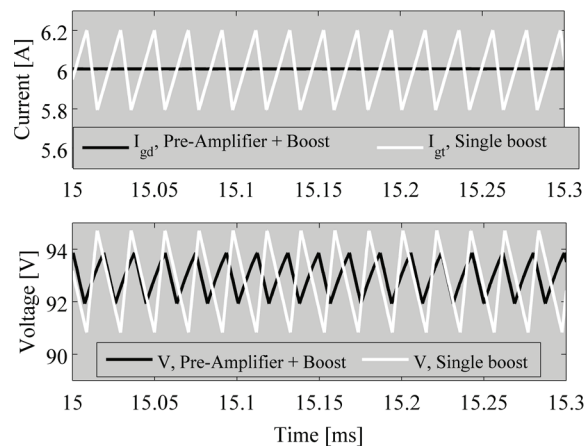
Figure 10 shows the simulation of the pre-amplifier based and single boost solutions. The waveforms of the pre-amplifier inductor currents and its input current, divided by two to allow its visualization in the same scale, are presented in figure 10(a). Such a simulation illustrates the complementary inductor current ripples, which interaction reduces the pre-amplifier input current ripple. The input current waveforms of the pre-amplifier based and single boost solutions are compared in the top of figure 10(b), which shows the significant reduction of the ripple injected to the source as described by (21).

Similarly, the reduction in the output voltage ripple in the pre-amplifier based solution, in comparison with the single boost solution, is depicted in the bottom of figure 10(b). Such an improvement is caused by the pre-amplifier voltage-boosting factor since in a boost converter the output voltage ripple depends on the difference between the input and output voltages.

The input current ripple ratio $\{100 \times \Delta I_{gd} / \Delta I_{dt}\}$ [%] is defined to quantify the reduction on the current ripple achieved by the pre-amplifier based solution over the single boost converter. Figure 11(a) shows the input current ripple ratio depending on the voltage conversion ratio $M(D)$ for different parasitic loss-resistance relations. It is observed that for $M(D) > 3$ the pre-amplifier strongly reduces the ripple injected to the source. In particular, considering $M(D) = 6$, the pre-amplifier based system generates only the 0.2 % of the single boost input current ripple.



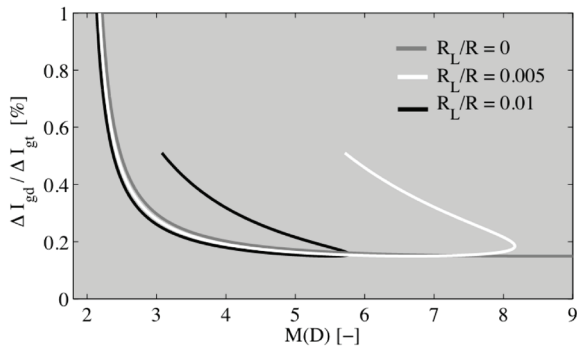
(a) Pre-Amplifier inductor currents



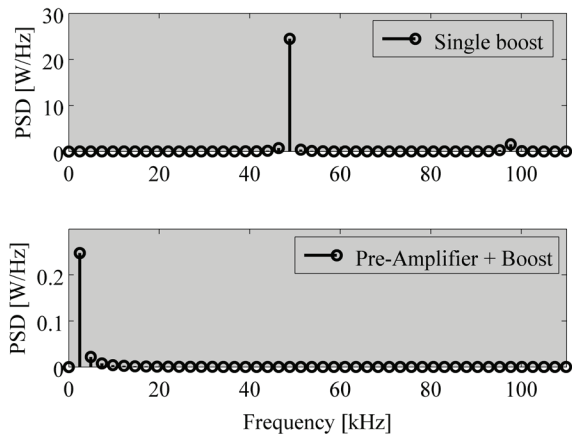
(b) Input current and output voltage ripples

Figure 10 Pre-Amplifier based and single boost systems waveforms

Figure 11(b) shows the Power Spectral Density (PSD) of the input current harmonics for both pre-amplifier based and single boost solutions. It is observed a large harmonic component at the switching frequency in the single boost solution, while the PSD of the pre-amplifier based solution does not exhibit such a component due to the complementary inductor currents operation. In addition, the scale used to plot the PSD of the proposed solution is 100 times smaller than the one adopted for the single boost, which makes evident the strong harmonics reduction achieved.



(a) Input current ripple ratio vs. conversion ratio



(b) Input currents harmonics content

Figure 11 Pre-Amplifier based and single boost systems current ripples magnitude

Experimental results

Experimental prototypes of the pre-amplifier based system, i.e. scheme of figure 7, and single boost solution, i.e. scheme of figure 1, have been developed to validate the analytical results. The inductors have been selected equal to 220 μH , the capacitors have been defined equal to 220 μF , obtaining a lumped parasitic resistances of 250 $\text{m}\Omega$ in each pre-amplifier branch and single boost converters. The load has been defined equal to 29.4 Ω , obtaining a parasitic losses ratio $R_L/R = 0.0085$, or 0.85 %, which is comparable with the one defined in the circuital simulations. The inductor and capacitor values have been

designed to achieve switching frequencies below 100 kHz and avoid electrolytic capacitors. The operating conditions have been defined by the input and output voltages $V_g = 12 \text{ V}$ and $V = 40 \text{ V}$, respectively.

Figure 12 shows the experimental waveforms of the inductors and input currents of the pre-amplifier converter. It is observed the opposite inductor currents slope as well as the small ripple in the input current, which corresponds to a 1.3 % of the DC component. In contrast, for the same operating conditions, the single boost solution produces an input current ripple equal to 12 % of the requested DC component.

Figure 13 presents the experimental efficiencies of both pre-amplifier based and single boost solutions. The pre-amplifier based solution exhibits an efficiency improvement of 7.7 % over the single boost case at $M(D) = 2$, and the efficiency difference grows until $M(D) = 3.5$ up to 10.1 % where the losses in the single boost limits the voltage boosting ratio in such classical solution. Instead, the pre-amplifier based system is able to supply higher voltage boosting ratios up to $M(D) = 5$. Such experimental results, which have been carried out at an output power range between 16 W and 125 W, demonstrate the ripple mitigation and efficiency improvement provided by the proposed pre-amplifier based system.

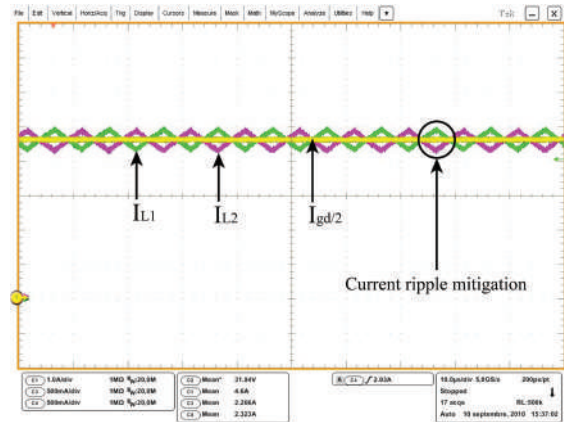


Figure12 Experimental pre-amplifier inductors and input current waveforms

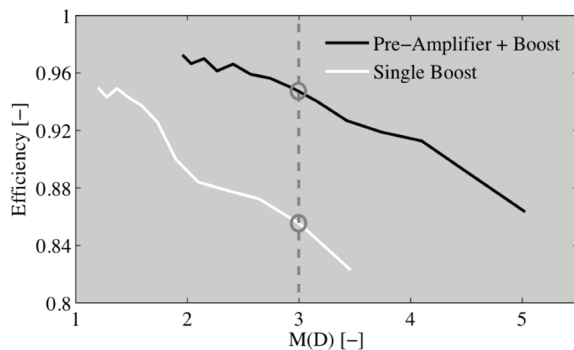


Figure 13 Experimental efficiency vs. conversion ratio of both proposed and classical solutions

Conclusions

This paper proposes a pre-amplifier aimed to reduce the current ripple injected to power sources by traditional DC/DC converters, being particularly analyzed with a boost converter. Besides, this solution improves the efficiency of the power conversion chain over the original system.

The proposed solution is based on interleaved boost converters, and it was analyzed in terms of efficiency and input current ripple. Its optimal operating conditions were calculated, and a sliding-mode controller was designed to ensure operation in such conditions.

The new power conversion chain, composed by the pre-amplifier and the original boost converter, was analyzed and contrasted with the original single boost solution. The theoretical analyses have been confirmed through PSIM circuital simulations, and experimental measurements validated the pre-amplifier benefits, obtaining a significant reduction up to 89 % of the original input current ripple, and an improvement on the efficiency between 7.7 % and 10.1 %.

Acknowledgments

This work was supported by GAUNAL and GITA research groups of the Universidad Nacional de Colombia (projects DACOGEN-PV

and MECOVA-WIND), the Spanish Ministerio de Ciencia e Innovación (project TEC2009-13172), and the Colombian Departamento Administrativo de Ciencia, Tecnología e Innovación COLCIENCIAS (scholarship 095-2005).

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