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Parallelogram Based Method for Space Vector Pulse Width Modulation

Modulación por Ancho de Pulso de Vectores Espaciales utilizando el Método del Paralelogramo

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Abstract

This paper presents a parallelogram based duty cycle computation method for space vector modulation control using standard pulse width modulation circuitry. This technique maps the voltage source inverter's solution space into only three parallelogram shaped zones and reduces the computational load. The proposed modulation methods are especially suited for a description of the voltage space vector in its α, β components and for modern and high dynamic applications, where demand changes may happen at a frequency comparable with the modulator carrier frequency. Several modulation methods used in scalar applications and extensively studied in the literature are easily obtained by combining the use of the modulation methods proposed in this work. The proposed methods have been validated by simulations and experimental test.

----- *Keywords:* Index Terms, PWM, inverters, DC-AC power conversion, space vector, space vector modulation, parallelogram.

Resumen

Este artículo presenta un método para la determinación del ciclo de trabajo de la modulación de vectores espaciales utilizando circuitos convencionales de modulación por ancho de pulso. Este método utiliza tres paralelogramos que cubren el espacio hexagonal de la salida del inversor, reduciendo de esta forma el esfuerzo de cálculo computacional. La metodología propuesta es aplicable directamente a la descripción de las componentes α, β del vector espacial en controladores modernos, con altos requerimientos dinámicos, donde la demanda de cambios se realiza a una frecuencia comparable con la

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de la señal portadora. Combinando las estrategias de modulación DPWMMIN y DPWMMAX propuestas en este trabajo, se obtiene fácilmente el ciclo de trabajo para otros métodos de modulación, utilizados en aplicaciones escalares y ampliamente estudiadas en la literatura. El método propuesto ha sido comprobado mediante simulaciones y ensayos experimentales.

----- *Palabras clave:* PWM, inversores, conversión de potencia CC-CA, vectores espaciales, modulación de vectores espaciales, paralelogramo

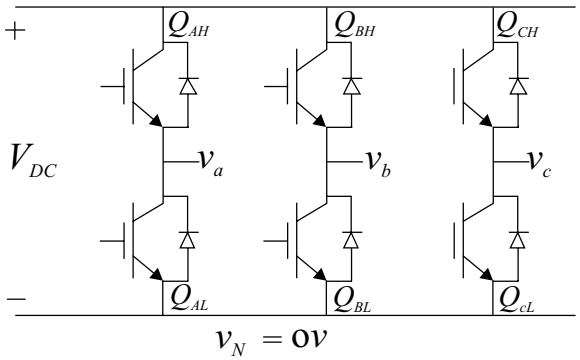
Introduction

The standard voltage source inverter (VSI), shown in figure 1a, can be found in many modern applications requiring precise control of power flow from AC to DC or vice versa, and much research has been devoted towards the development of efficient ways for controlling this type of converters [1-6]. From the many techniques used in the control of power converters, Pulse Width Modulation (PWM) has been in general the preferred choice, and over the past decades several variants of this technique have been studied. With the availability of new logic circuits of constantly increasing processing power, high performance control strategies based on space vector theory are possible, and Space Vector Pulse Width Modulation (SVPWM) seems especially suited for these and similar high dynamic control schemes. Although SVPWM has also been a subject of extensive research [7-22], there are few algorithms using the description of average voltages in natural (*a*, *b*, *c*) coordinates [19], an even less employing the description in (α, β) coordinates. In general, most of the published works deal with waveforms in quasi-steady state (per modulating period dynamics), where space vector advantages are not fully explored. In this work, an algorithm specially suited for applications requiring the generation of a per carrier period average voltage space vector in the (α, β) plane is proposed. This algorithm maps the inverter output voltage space state into three parallelogram sectors, as shown in figure 1b, covering the hexagonal shape of the locus of possible per carrier period average space vectors produced by the converter shown in figure 1(a). The proposed algorithm main advantage is a significant reduction in execution time during the computation of duty cycle demands for the PWM circuitry. For this, the duty cycle for each converter branch is obtained with a reduced number of arithmetic and logic operations and without using complex mathematical functions such as square roots, or trigonometric functions. The demanded average space vector $\vec{v}_s$ is synthesized using the triangle intersection technique, as in most PWM circuits. Seven modern modulation techniques are analyzed combining the use of Discontinuous Pulse Width Modulation Minimum and Maximum (DPWMMIN, DPWMMAX). The performance of the modulation methods is verified with experimental tests, and the results are presented in this paper.

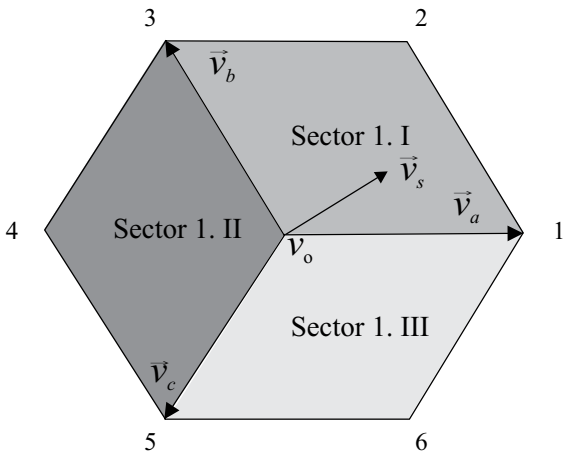
Methodology

Space vector modulation

The typical three-phase converter shown in figure 1(a) has $4^3 = 64$ possible states; of which only the $2^3 = 8$ states having a single power device turned "on" in each branch can be used in practice. Three of these states can be considered as a base to produce the remaining five states. Figure 1(b) shows the three base vectors $\vec{v}_a$, $\vec{v}_b$ and $\vec{v}_c$, corresponding to states (*1,0,0*), (*0,1,0*) and (*0,0,1*) respectively, and the hexagon vertices are identified by a number representing the bridge connectivity. In this representation a "1" corresponds to an upper power device turned "on" while the lower device is turned "off", and a "0" corresponds to a lower power device turned "on" while the upper device is turned "off".



(a) Voltage source inverter (VSI)



(b) Inverter output voltage space

Figure 1 Voltage source inverter (VSI) circuit diagram and output voltage space

Any average voltage space vector inside the hexagonal shape shown in figure 1(b) can be obtained by using the Clarke transformation:

$$\vec{v} = v_\alpha + jv_\beta = c(v_a + \alpha v_b + \alpha^2 v_c)$$
$$= c\left[(v_a - v_N) + \alpha(v_b - v_N) + \alpha^2(v_c - v_N)\right] \quad (1)$$
$$= cV_{DC}\left(D_a + \alpha D_b + \alpha^2 D_c\right)$$

Where $\alpha = e^{j\frac{2\pi}{3}}$, and D_a, D_b, D_c, are the duty cycles for each inverter branch; c usually takes the values 1, ⅔ or $\sqrt{2/3}$.

In the three phase coordinates, the three base vectors are α_1, α_2 and α_3, of unitary magnitude; each phase generates a spatial vector in the corresponding direction, whose magnitude is found to be $|\vec{v}_a| = |\vec{v}_b| = |\vec{v}_c| = cV_{DC}$ (c is a scale factor set by the mathematical transformation used in the vector calculation), and with Pulse Width Modulation during a carrier signals period, each branch average voltage can be modified. Since the zero vector can be synthesized using states (*0,0,0*) or (*1,1,1*), there are in theory infinite possible combinations to synthesize an average voltage space vector using standard triangular carrier modulators. As a consequence of this large amount of possible combinations for synthesizing voltage space vectors, SVPWM can be found in the literature under different names [12, 13, 23]. To simplify the analysis, in this work three possible methods are used to synthesize any space vector in the hexagonal locus covered by the base vectors using carrier based modulation, usually known as Discontinuous Pulse Width Modulation Minimum (DPWMMIN), Discontinuous Pulse Width Modulation Maximum (DPWMMAX) and SVPWM in the literature [12]. However, there are other switching strategies, such as sequences type III and type IV [21], or special sequences for ripple minimization that are not suitable for standard triangular carrier implementations [18, 21, 24].

Discontinuous PWM minimum (DPWMMIN)

In DPWMMIN [12, 23], the desired average voltage space vector $\vec{v}_s = v_\alpha + jv_\beta$ is synthesized by adjusting the two neighboring base vectors magnitude with PWM and at the same time setting the remaining base vector to zero; in this case the zero vector is produced with state (*0,0,0*). Figure 1(b) shows the three parallelograms defining three different sectors used in the synthesis of any average voltage space vector $\vec{v}_s$ in the hexagonal space vector locus. Figure 2 shows the decomposition of a space vector $\vec{v}_s$ in sector 1.I. In this case $D_{1b} \cdot \Im m(\vec{v}_b)$ produces the β component of $\vec{v}_s$ and $D_{1b} \cdot \Re e(\vec{v}_b)$ produces the vector component $\Delta\vec{v}_{s\alpha}$ that needs to be compensated with part of base vector $\vec{v}_a$.

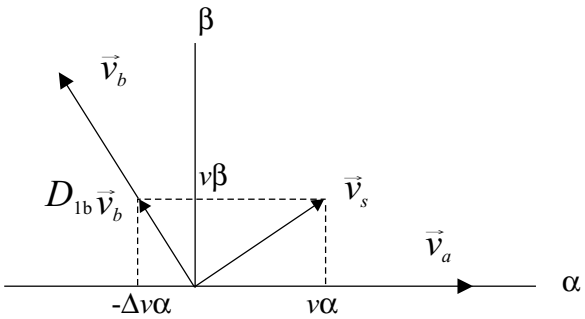


Figure 2 Decomposition $\vec{v}_s$ of in sector 1.I using the DPWMMIN modulation system

By using the following auxiliary variables:

$$\left.\begin{aligned}\zeta_1 &= \frac{v_{s\alpha}}{cV_{DC}} \\ \zeta_2 &= \frac{v_{s\beta}}{c\sqrt{3}V_{DC}}\end{aligned}\right\} \quad (2)$$

The equations defining the duty cycles required to synthesize any average voltage space vector using DPWMMIN as a function of the parallelogram sectors shown in figure 1(b), are:

1) Sector 1.I:

$$\left.\begin{aligned}D_{1a} &= \zeta_1 + \zeta_2 \\ D_{1b} &= 2\zeta_2 \\ D_{1c} &= 0\end{aligned}\right\} \quad (3)$$

2) Sector 1.II:

$$\left.\begin{aligned}D_{1a} &= 0 \\ D_{1b} &= -\zeta_1 + \zeta_2 \\ D_{1c} &= -\zeta_1 - \zeta_2\end{aligned}\right\} \quad (4)$$

3) Sector 1.III:

$$\left.\begin{aligned}D_{1a} &= \zeta_1 - \zeta_2 \\ D_{1b} &= 0 \\ D_{1c} &= -2\zeta_2\end{aligned}\right\} \quad (5)$$

The sector selection algorithm for DPWMMIN is presented in Table 1.

Table 1 Sector selection algorithm for DPWMMIN modulation using the proposed method.

Program step	*Use D_{1a}, D_{1b}, D_{1c} defined by equation:*	*Sector selected:*
if $(\lvert\zeta_2\rvert < -\zeta_1)$ then	(4)	1.II
else if $\zeta_2 > 0$ then	(3)	1.I
else	(5)	1.III
end if		

Figure 3 shows an example of the control signals that must be applied to the power devices in each branch when a PWM with central symmetry is used to synthesize a space vector with this modulating strategy. In this example the average voltage space vector reference is in sector 1.III and the resulting instantaneous VSI vector sequence is $\vec{v}_6 \rightarrow \vec{v}_5 \rightarrow \vec{v}_0 \rightarrow \vec{v}_5 \rightarrow \vec{v}_6$ for $D_{1c} > D_{1a}$; the null vector $\vec{v}_0$ is synthesized with state (*0,0,0*).

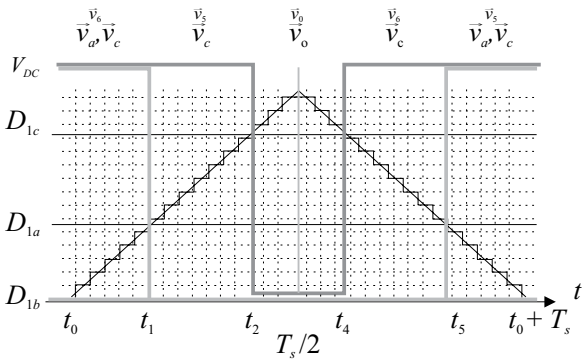


Figure 3 Firing sequence for a PWM with central symmetry, DPWMMIN modulation method

Discontinuous PWM maximum (DPWMMAX)

In DPWMMAX [12, 23], the base space vector closer to the space vector to be synthesized is

turned "on", and the magnitude of the remaining two base space vectors is adjusted with PWM; in this case zero vector v_0 is produced with state (*1,1,1*) [13].

Figure 4 shows the three parallelograms defining three different sectors used in DPWMMAX to synthesize any average voltage space vector $\vec{v}_s$, and figure 5 shows the decomposition of a space vector $\vec{v}_s$ in sector 2.II. In this case the effect of turning "on" branch *c* during the whole switching period is that phases *a* and *b* have to synthesize space vector $\vec{v}_s'$, obtained with the following expression:

$$\begin{aligned}\vec{v}' &= \vec{v} - \vec{v}_c = v'_\alpha + jv'_\beta \\ &= (v_\alpha + \tfrac{1}{2}cV_{DC}) + j(v_\beta + \tfrac{\sqrt{3}}{2}cV_{DC})\end{aligned} \quad (6)$$

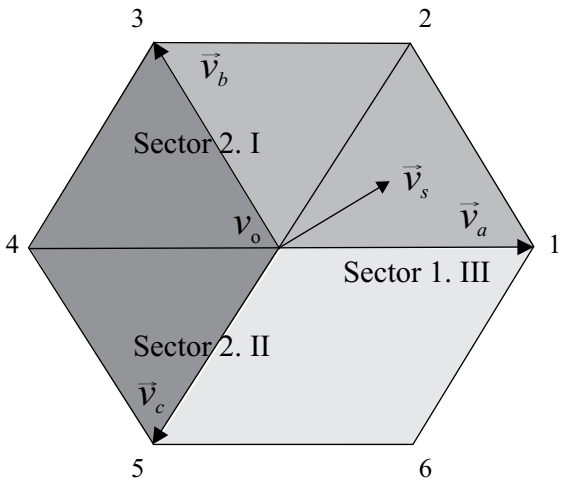


Figure 4 Base space vectors and parallelogram sectors for DPWMMAX

In general, the equations defining the duty cycles required to synthesize any vector using DPWMMAX as a function of the sectors shown in figure 4 are:

1) Sector 2.I:

$$\left.\begin{aligned} D_{2a} &= 1 + \zeta_1 - \zeta_2 \\ D_{2b} &= 1 \\ D_{2c} &= 1 - 2\zeta_2 \end{aligned}\right\} \quad (7)$$

2) Sector 2.II:

$$\left.\begin{aligned} D_{2a} &= 1 + \zeta_1 + \zeta_2 \\ D_{2b} &= 1 + 2\zeta_2 \\ D_{2c} &= 1 \end{aligned}\right\} \quad (8)$$

3) Sector 2.III:

$$\left.\begin{aligned} D_{2a} &= 1 \\ D_{2b} &= 1 - \zeta_1 + \zeta_2 \\ D_{2c} &= 1 - \zeta_1 - \zeta_2 \end{aligned}\right\} \quad (9)$$

The sector selection algorithm for DPWMMAX is presented in table 2.

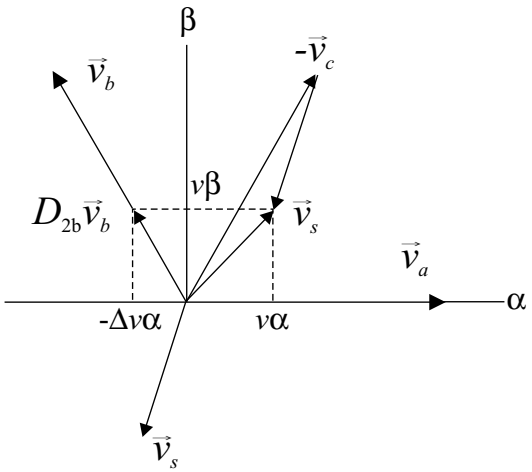


Figure 5 Decomposition of $\vec{v}_s$ in sector 2.II using the DPWMMAX modulation system

Table 2 Sector selection algorithm for DPWMMAX modulation using the proposed method

Program step	*Use D_{1a}, D_{1b}, D_{1c} defined by equation:*	*Sector selected:*
if $(\lvert\zeta_2\rvert < \zeta_1)$ then	(9)	2.III
else if $\zeta_2 > 0$ then	(7)	2.I
Else	(8)	2.II
end if		

Figure 6 shows an example of the control signals that must be applied to the power devices in each branch when a PWM with central symmetry is used to synthesize a space vector with this modulating strategy. In this example the vector to synthesize is in sector 2.I and the resulting instantaneous VSI vector sequence is $\vec{v}_7 \rightarrow \vec{v}_4 \rightarrow \vec{v}_3 \rightarrow \vec{v}_4 \rightarrow \vec{v}_7$ for $D_{2c} > D_{2a}$; the null vector $\vec{v}_0$ is synthesized with state (*1,1,1*).

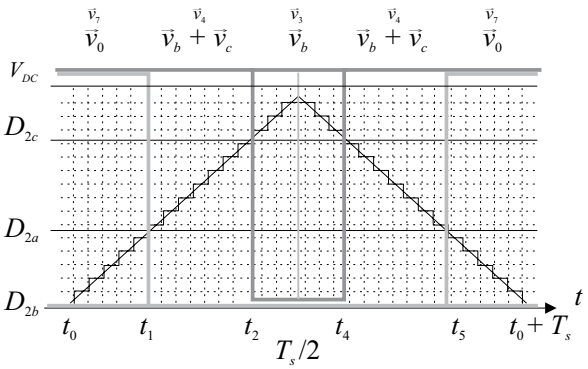


Figure 6 Firing sequence for a PWM with central symmetry, DPWMMAX method

Space Vector Pulse Width Modulation (SVPWM)

In SVPWM [12, 23] the duty cycle defining the conduction of the power devices in each branch is obtained by averaging the duty cycle obtained using DPWMMIN and DPWMMAX. In this way, zero vector v_0 is synthesized with both states (*0,0,0*) and (*1,1,1*) [13]; in a more general form, the duty cycle is computed using the following equations.

$$\left.\begin{aligned} D_{3a} &= \delta_1 D_{1a} + \delta_2 D_{2a} \\ D_{3b} &= \delta_1 D_{1b} + \delta_2 D_{2b} \\ D_{3c} &= \delta_1 D_{1c} + \delta_2 D_{2c} \\ 1 &= \delta_1 + \delta_2 \end{aligned}\right\} \qquad (10)$$

Figure 7 shows an example of the control signals that must be applied to the power devices in each branch when a PWM with central symmetry is used to synthesize a space vector with this modulating strategy. In this example the space vector is synthesized with base vectors $\vec{v}_b$ and $\vec{v}_c$, and the resulting instantaneous VSI vector sequence is $\vec{v}_7 \rightarrow \vec{v}_4 \rightarrow \vec{v}_3 \rightarrow \vec{v}_0 \rightarrow \vec{v}_3 \rightarrow \vec{v}_4 \rightarrow \vec{v}_7$ for $D_{3b} > D_{3c} > D_{3a}$. The relative size of constants δ_1 and δ_2 used to synthesize v_0 define the relative duration in time of states (*0,0,0*) and (*1,1,1*). Figure 7 shows the case when $\delta_1 = \delta_2 = 0.5$.

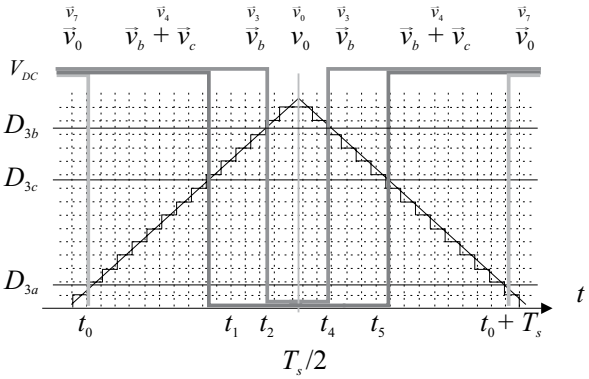


Figure 7 Firing sequence for a PWM with central symmetry, SVPWM method

Figures 8(a) to 8(c) show the typical duty cycles required to produce a maximum amplitude circular trajectory of the voltage space vector for the three previously discussed methods [25]. The circular trajectory is modeled in the (α, β) plane using the following expressions:

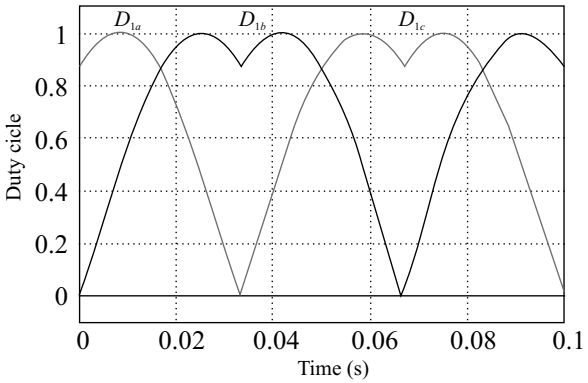
$$v_\alpha(t) = \frac{\sqrt{2}}{2} V_{DC} \cos \omega t \qquad (11)$$

$$v_\beta(t) = \frac{\sqrt{2}}{2} V_{DC} \sin \omega t \qquad (12)$$

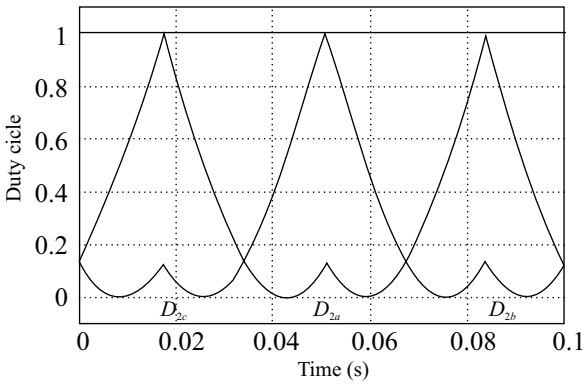
Generalized modulation algorithm

As mentioned previously, the number of modulation methods is in theory infinite, depending on δ_1 and δ_2 values, but only few have been reported in practical applications [26]. In general the modulation methods are divided in continuous PWM (CPWM) and discontinuous PWM (DPWM). The methods proposed in this work can be adapted to those presented in [12],

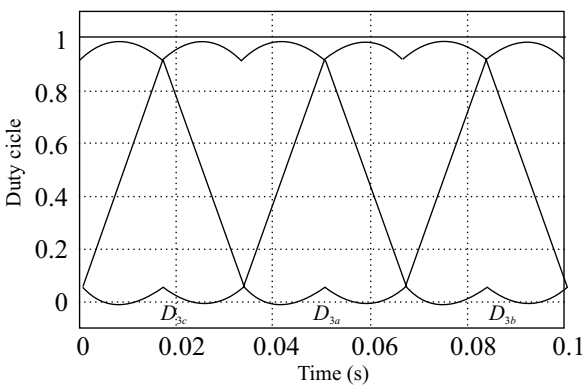
by setting the values for δ_1 and δ_2 depending on the angle θ of the demanded inverter voltage $\vec{v}$.



(a) DPWMMIN



(b) DPWMMAX



(c) SVPWM

Figure 8 Modulation waveform for a maximum amplitude circular trajectory of the inverter voltage space in SVPWM with $\delta_1 = \delta_2 = 0.5$

It was established previously that SVPWM is obtained with $\delta_1 = \delta_2 = 0.5$; DPWM0, DPWM1, DPWM2 and DPWM3 are obtained as follows:

A. DPWM0 is obtained by setting:

$$\delta_1 = 1, \quad \delta_2 = 0 \quad if \quad \left\{ \begin{array}{l} 0 \le \theta \le \frac{\pi}{3} \\ \frac{2\pi}{3} \le \theta \le \pi \\ \frac{4\pi}{3} \le \theta \le \frac{5\pi}{3} \end{array} \right\} \quad (13)$$
$$\delta_1 = 0, \quad \delta_2 = 1 \quad otherwise$$

B. DPWM1 is obtained by setting:

$$\delta_1 = 1, \quad \delta_2 = 0 \quad if \quad \left\{ \begin{array}{l} \frac{\pi}{6} \le \theta \le \frac{\pi}{2} \\ \frac{5\pi}{6} \le \theta \le \frac{7\pi}{6} \\ \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \end{array} \right\} \quad (14)$$
$$\delta_1 = 0, \quad \delta_2 = 1 \quad otherwise$$

C. DPWM2 is obtained by setting:

$$\delta_1 = 0, \quad \delta_2 = 1 \quad if \quad \left\{ \begin{array}{l} 0 \le \theta \le \frac{\pi}{3} \\ \frac{2\pi}{3} \le \theta \le \pi \\ \frac{4\pi}{3} \le \theta \le \frac{5\pi}{3} \end{array} \right\} \quad (15)$$
$$\delta_1 = 1, \quad \delta_2 = 0 \quad otherwise$$

D.- DPWM3 is obtained by setting:

$$\delta_1 = 0, \quad \delta_2 = 1 \quad if \quad \left\{ \begin{array}{l} \frac{\pi}{6} \le \theta \le \frac{\pi}{2} \\ \frac{5\pi}{6} \le \theta \le \frac{7\pi}{6} \\ \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \end{array} \right\} \quad (16)$$
$$\delta_1 = 1, \quad \delta_2 = 0 \quad otherwise$$

Experimental results

The proposed algorithm was implemented on a custom build floating point DSP (ADSP-21061-40 MHz) based test-rig [27]. The power stage shown in figure 1(a) uses six 50A, 1200V, IGBTs, with a 2200 μF 450 V capacitor in the DC link. The load is made of three star connected inductors with L=7.0 mH, and R=0.05 Ω. The PWM signals are obtained from a motion coprocessor ADMC-201AP with the following operating conditions:

Clock Frequency: 8 MHz

Dead time: 500 ns

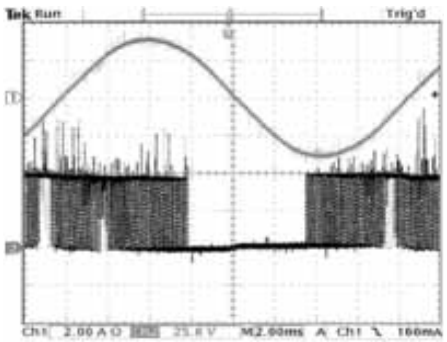
Pulse deletion: 500 ns

PWM master switch period selection: 800

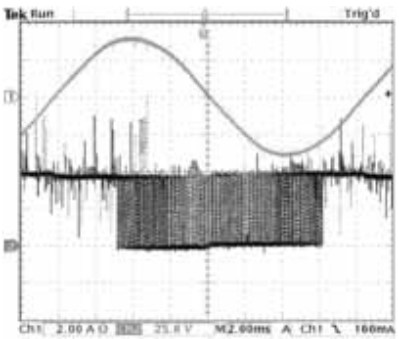
With this set up the PWM circuitry is operating at 10 kHz switching frequency, and the registers for programming the PWM duty cycles use integers in the range [0 to 800] for duty cycles between 0% and 100%. Figures 9 to 12 show the current, trigger signal and current harmonics content for phase "*a*" when the modulation methods DPWMMIN, DPWMMAX, DPWM0, DPWM1, DPWM2 and DPWM3 are applied to the power converter for a circular trajectory in the linear region with (MI=0.898). In general, as was to be expected, the current waveforms and harmonics content are almost the same in the six implemented modulation methods, but the trigger signals have different characteristics.

Conclusions

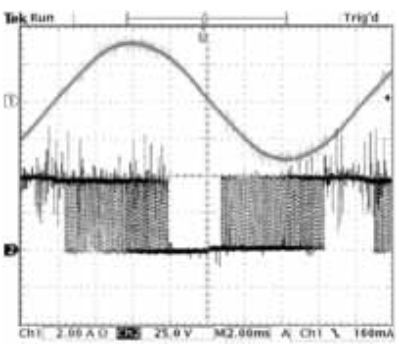
Three basic methods, DPWMMIN, DPWMMAX and SVPWM using a parallelogram based mapping algorithm for producing per phase duty cycles, for references in α, β coordinates have been proposed, and experimental results for DPWMMIN and DPWMMAX and other four combined methods, DPWM0, DPWM1, DPWM2 and DPWM3 have been presented in this work. The proposed modulation methods are especially suited for controllers requiring high dynamic response such as FOC, DTC, DPC, etc., and are easily adapted to be used in scalar controllers. An advantage of the proposed methods is that they employ the triangle intersection technique and the resulting duty cycles can be readily fed to standard carrier-based PWM modules.



(a) DPWMMIN

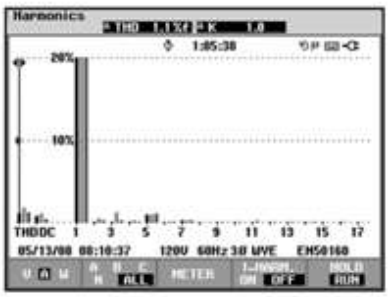


(b) DPWMMAX

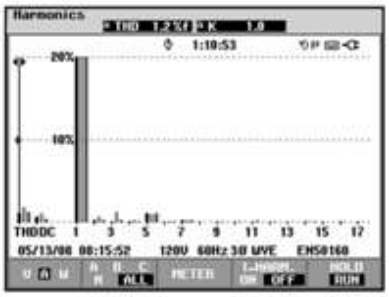


(c) DPWMO

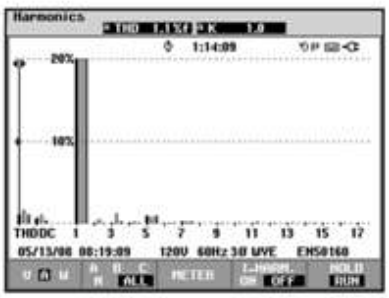
Figure 9 Experimental phase "*a*" current and power devices' trigger signal for DPWMMIN, DPWMMAX and DPWM0 modulation methods implemented using the proposed algorithms



(a) DPWMMIN

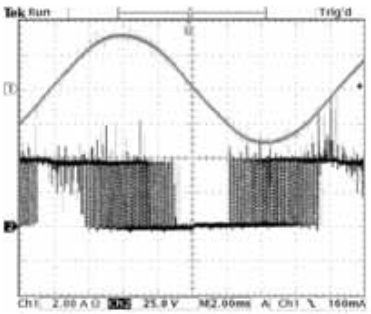


(b) DPWMMAX

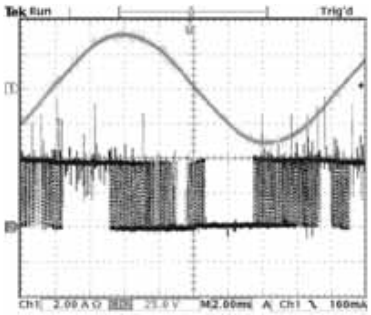


(c) DPWMO

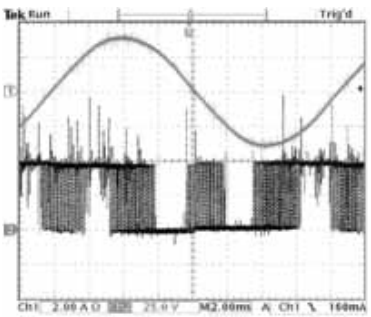
Figure 10 Experimental phase "*a*" current harmonics content for DPWMMIN, DPWMMAX and DPWM0 modulation methods implemented using the proposed algorithms



(a) DPWM1



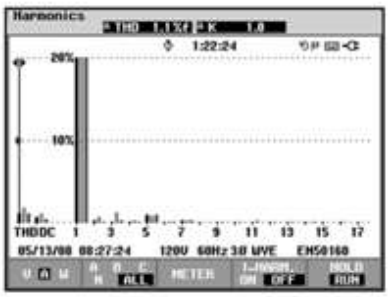
(b) DPWM2



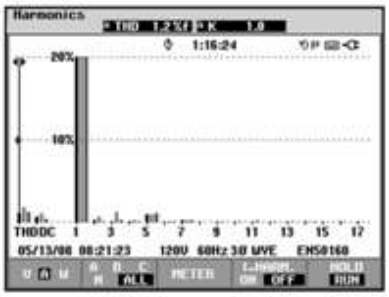
(c) DPWM3

Figure 11 Experimental phase "*a*" current and power devices' trigger signal for DPWM1, DPWM2 and DPWM3 modulation methods implemented using the proposed algorithms

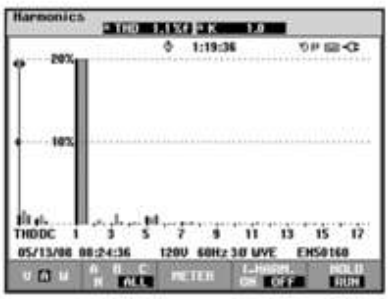
The mathematical operations required by the algorithms are simple multiplications, additions, absolute values and comparisons, making them suitable to be implemented in low performance processors. The algorithms run in less than 2μs, using less than 2% of the control cycle defined in the test rig DSP controller [27]. This is a very important advantage when the proposed modulation strategies are used in modern applications where the overall control scheme represents a high computational load. Several modern modulation techniques can be obtained combining the use of DPWMMIN and DPWMMAX by properly selecting the areas for using each method. This approach also leads to a reduction in the computational burden of these modern modulation methods. The performance of the modulation methods has been verified with experimental tests, and the results are in good agreement with the theoretical analysis presented in this paper.



(a) DPWM1



(b) DPWM2



(c) DPWM3

Figure 12 Experimental phase "*a*" current harmonics content for DPWM1, DPWM2 and DPWM3 modulation methods implemented using the proposed algorithms

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