Efficient hardware implementation of a full COFDM processor with robust channel equalization and reduced power consumption

Implementación eficiente en hardware de un procesador COFDM completo con ecualización de canal robusta y reducción de consumo de potencia

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Abstract

This work presents the design of a 12 Mb/s Coded Orthogonal Frequency Division Multiplexing (COFDM) baseband processor for the standard IEEE 802.11a. The COFDM baseband processor was designed by using our designed circuits for carrier phase correction, symbol timing synchronization, robust channel equalization and Viterbi decoding. These circuits are flexible, parameterized and described by using generic structural VHDL. The COFDM processor has two clock domains for reducing power consumption, it was synthesized on a Stratix II FPGA, and it was experimentally tested by using 2.4 GHz Radio Frequency (RF) circuitry.

---------- *Keywords:* OFDM, field programmable gate arrays (FPGAs), radio frequency, receivers, channel coding, channel estimation

Resumen

Este trabajo presenta el diseño de un procesador banda-base para multiplexación por división de frecuencias ortogonales codificada (COFDM) de 12 Mb/s para el estándar IEEE 802.11a. El procesador COFDM banda-base fue diseñado usando circuitos diseñados por nosotros para corrección de

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fase de portadora, sincronización de tiempo de símbolo, ecualización de canal robusta y decodificación Viterbi. Estos circuitos son flexibles, parametrizados y descritos usando VHDL estructural y genérico. El procesador COFDM banda-base tiene dos dominios de reloj para reducción del consumo de potencia, fue sintetizado sobre un FPGA Stratix II y fue probado experimentalmente usando circuitería de radio frecuencia (RF) a 2.4 GHz.

---------- *Palabras clave:* OFDM, FPGAs, radio frecuencia, receptores, codificación de canal, estimación de canal

Introduction

Most modern wireless digital communication systems use OFDM for modulation and multiplexation, because it has reliable performance on noisy and multipath channels with selective fading [1], these channels are typical on mobile environments. Some systems that use OFDM are: Wireless Local Area Networks (WLANs) [2], Terrestrial Digital Video Broadcasting (DVB) [3], emerging Cognitive Radio standards for Wireless Regional Area Networks (WRANs) [4], Long Term Evolution (LTE) for mobile communications [5], Power Line Communications (PLC) [6], Digital Subscriber Line (DSL) services [7], among others. These OFDM communications systems require bandwidths ranging from 1.25 MHz to 20 MHz, time and phase synchronization, and channel equalization, additionally reduced power consumption is desired; thus it is necessary to design efficient hardware architectures for COFDM processors. In this context, in the literature there are several works about baseband architectures for OFDM transmitter [8-10] and receiver [11-16] on FPGA platforms, mostly of them use single clock domain and in [16] gated clock domains are used in the receiver. Nevertheless, several research works have focused their interest around the symbol timing synchronization, carrier synchronization and channel equalization issues on OFDM communication systems [11, 16-18]. However, in the reviewed literature we did not find a hardware implementation of a full COFDM baseband processor with two clock domains in the receiver and in the transmitter which includes channel coding, channel equalization, phase correction and the RF interface. Therefore, this paper presents the design of a full COFDM baseband processor with channel equalization and reduced power consumption by using two clock domains.

This paper is organized as follows: First, some COFDM concepts are described, then the design of baseband processor architecture is presented and its functional blocks are described, later the in-system hardware verification results are discussed, and finally the conclusions are presented.

COFDM concepts

OFDM is a multicarrier scheme for telecommunication systems that allows modulation of N parallel data streams with N orthogonal sub-carriers. An OFDM signal is described by Eq. (1) [1].

$$s(t) = \frac{1}{\sqrt{T_s}} \sum_{k=-N/2}^{k=N/2} s_k \exp\left(\frac{j2\pi kt}{T_s}\right) \Pi\left(\frac{t}{T_s} - \frac{1}{2}\right) \quad (1)$$

Where s_k is the k-th data stream composed by complex symbols obtained from an M-ary mapping process, T_s is the time of the OFDM signal, and N is the number of sub-carriers. From Eq. (1) it can be seen that sub-carriers are orthogonal, due to this, OFDM does not require guard bands [1]. Each data stream s_k is generated with a low symbol rate, which minimizes the selective fading effects of multipath channels [1]. By discretizing $s(t)$ with $t = nT$ and $T_s = NT$ in Eq. (1), we get Eq. (2).

$$s[n] = \frac{1}{\sqrt{NT}} \sum_{k=-N/2}^{k=N/2} s_k \exp\left(\frac{j2\pi kn}{N}\right), \quad -N/2 \le n \le N/2 \quad (2)$$

Where, $s[n]$ is the OFDM symbol, n is the discrete time index and T is the sampling time of sub-carriers; $s[n]$ is computed by performing the Inverse Discrete Fourier Transform (IDFT) of s_k; then, the OFDM modulation is carried out by using the IDFT of M-ary symbols in the transmitter, and the OFDM demodulation is carried out by using the DFT of received signal in the receiver. Also, the receiver requires performing synchronization and equalization tasks before the DFT processing. However, Fast Fourier Transform (FFT) algorithms are used for OFDM.

Additionally, OFDM includes a cyclic prefix to minimize the effects of multipath channels, one of these effects is the loss of orthogonality that increases Inter Symbol Interference (ISI) [1]. The cyclic prefix is the last Δ samples of $s[n]$, and it is appended at the beginning of $s[n]$, thus an OFDM symbol with cyclic prefix has $N+\Delta$ samples.

When channel coding for Forward Error Correction (FEC) is included in the OFDM system [1], the result is a COFDM system; typical FEC techniques used in COFDM systems are Convolutional Coding [2], Reed-Solomon Coding and Turbo Coding [4].

There are four tasks that make COFDM receiver more complex than the COFDM transmitter: Timing synchronization, carrier synchronization, channel equalization and FEC decoding. Timing synchronization is performed by detecting the presence of a COFDM symbol on the channel and by estimating the index time of the payload data. Carrier synchronization is the correction of the frequency and phase mismatches between local oscillators in the transmitter and the receiver. Channel equalization is an adaptive estimation of the transfer function of the RF channel. FEC decoding is accomplished by the Viterbi algorithm [19, 20].

The standard IEEE 802.11a defines a WLAN based on COFDM that operates in the 5 GHz band [2]. This standard allows bit rates up to 54 Mb/s and a bandwidth of 20 MHz. The COFDM symbol is obtained by using an FFT of N=64 points and a cyclic prefix of Δ=*16* samples; thus, an OFDM symbol has a time of *(64+16)/20 MHz = 4* μs. From the 64 sub-carriers, only 48 sub-carriers are used for data, 4 sub-carriers as pilots and the remaining 12 sub-carries keep on zero [2]. The maximum allowed symbol rate is 48/4 μs = 12 Ms/s. Figure 1 shows the block diagram of physical layer (PHY) defined on the IEEE 802.11a standard [2].

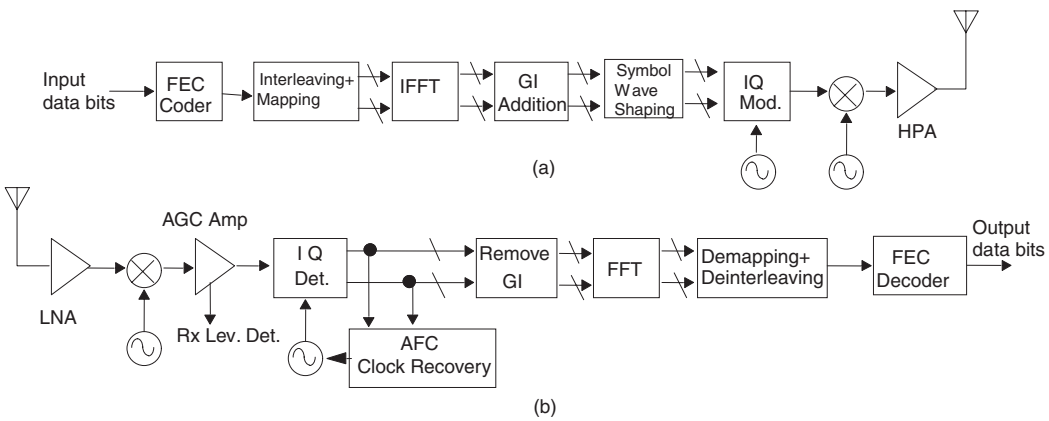


Figure 1 Block diagram of IEEE 802.11a PHY, (a) Transmitter, (b) receiver, taken from [2]

The FEC coding in the transmitter is implemented by using a convolutional encoder with *K=7* and *r=1/2* [2]. The short preamble sequence $p_s[n]$ and the long preamble sequence $p_l[n]$ are transmitted before a set of *s[n]* symbols [2], this allows the synchronization and equalization tasks in the

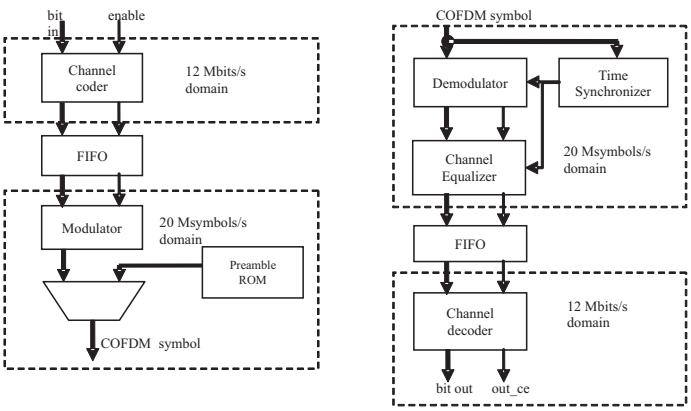
receiver; nonetheless, IEEE 802.11a does not describe the way to implement them.

Design of the COFDM baseband processor

From the COFDM PHY layer defined on standard IEEE 802.11a [2], we designed a full COFDM baseband processor by using two clock domains, one of 12 MHz for channel coding and mapping of bits and one of 20 MHz for FFT based modulation of symbols; this approach avoids to use a 60 MHz (least common multiple between 12 and 20) single clock domain, which increases the power consumption. Transfers between clock domains are accomplished through asynchronous First In First Out (FIFO) modules. The proposed clock domains allow achieving a high performance and reduced power consumption. Next we present a general description of the COFDM baseband processor and the design of the functional blocks by considering novel designs for symbol detection and channel equalization.

Description of the COFDM baseband processor

Figure 2 shows a simplified block diagram of the COFDM baseband processor for the transmitter and the receiver.



(a) Transmitter (b) Receiver

Figure 2 Block diagram of the COFDM baseband processor

The COFDM transmitter in figure 2(a) is composed of a channel coder; a modulator; an asynchronous FIFO, which is a gateway between the channel coder and the modulator; a multiplexer; and a Read Only Memory (ROM) that stores the short and long preamble sequences, which are used jointly with the pilot sub-carriers to perform synchronization and channel equalization tasks in the receiver.

The channel coder performs the convolutional encoding and interleaving of a 12 Mb/s stream segmented into 48-bit packets, and the interleaved di-bits are mapped into 48 Quadrature Phase Shift Keying (QPSK) symbols with a rate of 12 Msymbols/s.

The modulator performs a 64-point IFFT (Inverse FFT) by using 48 mapped symbols, 4 pilot sub-carriers and 12 zero sub-carriers; and this appends the 16-point cyclic prefix to generate the 80-samples COFDM symbol with a rate of 20 Msamples/s and a time of $4\ \mu s$.

The COFDM receiver in figure 2(b) is composed of a time synchronizer, a demodulator, a channel equalizer, a channel decoder, and an asynchronous FIFO, which is a gateway between the channel equalizer and the channel decoder. The time synchronizer estimates the COFDM symbol time by using two correlators, the first one is a short-preamble auto-correlator for symbol detection, and the second one is a

long preamble cross-correlator for symbol time estimation. The demodulator removes the cyclic prefix and performs a 64-point FFT. The channel equalizer corrects the phase mismatch between the sub-carriers of the COFDM transmitter and receiver, and it estimates the transfer function of the channel; the phase mismatch is estimated from the received pilot sub-carriers, and the channel transfer function is estimated by using the DFT of the long preamble sequence. The channel decoder performs the de-mapping of the 48 QPSK symbols by using their sign bits, the de-interleaving, and the Viterbi decoding that recovers the 48 data bits.

Hardware implementation of functional modules

Convolutional encoder and Viterbi decoder modules

The convolutional encoder in the transmitter is based on Linear Feedback Shift Registers (LFSRs), and its parameters are: constraint length K = 7, rate r = 1/2, and generator polynomials g0 = 133o and g1 = 171o. The Viterbi decoder in the receiver is implemented by using hard decision approach and double-buffer architecture. Figure 3 shows the designed Viterbi decoder.

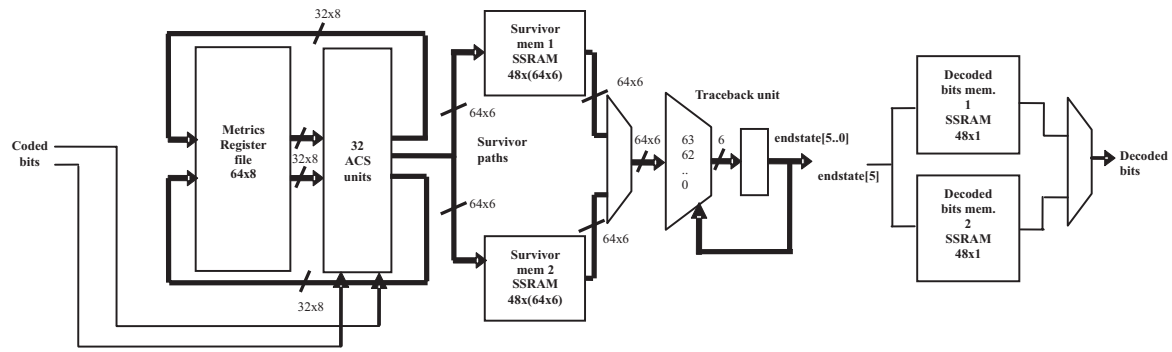


Figure 3 Viterbi decoder

The designed Viterbi decoder has 32 Add Compare Select (ACS) units, a 64x8 register file, a traceback unit, a double-buffer stage for the survivor paths by using 48x(64x6) Synchronous Static Random Access Memories (SSRAMs), and a double-buffer stage for the decoded bits by using 48x1 SSRAMs. The ACS units compute the accumulated metrics and the survivor path for each state [20]. The register file stores the accumulated metrics for each state. The traceback unit starts the decoding from the zero state because the last 6 bits of each transmitted data frame are zero. The pipelined double-buffer stages achieve a throughput of 1 decoded bit per clock cycle. In the transmitter and receiver, the encoded bits are interleaved and de-interleaved by implementing the first permutation defined on [2] by using mod-16 arithmetic.

QPSK mapping and de-mapping modules

The QPSK mapping module in the transmitter maps interleaved di-bits to QPSK symbols with unitary power by using the QPSK constellation shown in figure 4(a), where A= $\sqrt{2}/2$. The QPSK mapper is designed by using a Look Up Table (LUT) with two entries as shown in figure 4(b).

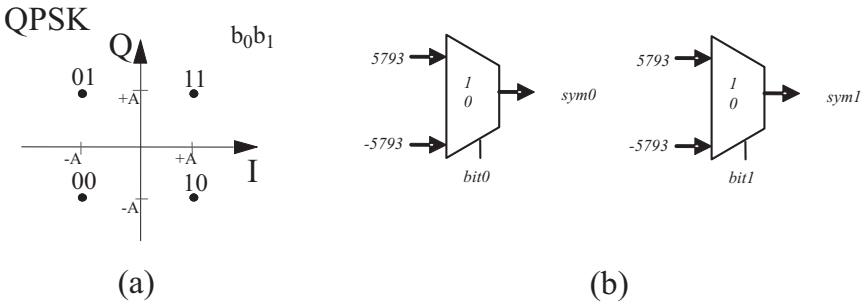


Figure 4 QPSK Constellation (a), QPSK mapper (b)

The value $\sqrt{2}/2$ is hardwired by using a 14-bit fixed point representation with 13 fractional bits. The QPSK de-mapping module in the receiver de-maps the QPSK symbols to di-bits by finding the quadrant in the complex plane, where the received symbol is located; the sign bit of *I* and *Q* allows this operation.

IFFT/FFT modules

The IFFT module in the transmitter and the FFT module in the receiver are based on the 64-point R2^{2}SDF architecture [21]. In this case, we modified this architecture by adding pipeline stages, a rounding hardware that implements the nearest-even approach, and a bit-reversing module that uses a double-buffer structure. In the transmitter an additional module is designed to generate the cyclic prefix. The operation of the FFT module in the receiver is started by the long preamble cross-correlator when it detects the first sample of the COFDM symbol after the cyclic prefix. A COFDM symbol is composed by 80 samples and its time is 4 μs for a 20-MHz clock signal.

Timing synchronization modules

The timing synchronization modules detect the COFDM symbol and estimate the timing of data packets in time domain before demodulation. The detection of the COFDM symbol is accomplished by a short preamble auto-correlation circuit [22]. The timing estimation of data packets is accomplished by a long preamble cross-correlation circuit [14]. In figure 5 is shown the designed short preamble auto-correlator, which has less number of delay elements than the circuits presented in [14, 15].

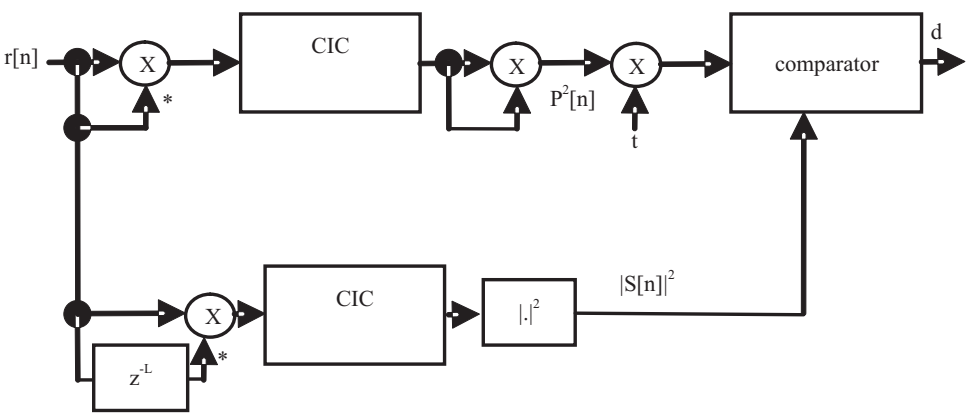


Figure 5 Short preamble correlator

The short preamble correlator is a delayed auto-correlation circuit, which detects periodic signals with period $T = L$. In this case, L=16 is the fundamental period of the short preamble

sequence [2]. The upper branch computes the squared energy $P^2[n]$ of the incoming signal $r[n]$ on a sliding window of L samples. The lower branch computes the squared magnitude $|S[n]|^2$ of the auto-correlation between $r[n]$ and the $r[n - L]$ on a sliding window of L samples. The sliding window is implemented by using Cascaded Integrator Comb (CIC) modules [14, 15]. A COFDM symbol is detected when the equation (3) is true.

$$|S[n]|^2 \geq tP^2[n] \quad (3)$$

Where, t is the threshold, which is calculated from the Signal to Noise Ratio (SNR) of the channel and it has a value near to unity of the form $t = (2^l - 1) / 2^l$, this allows representing the product $tP^2[n]$ as $P^2[n] - P^2[n] >> l$.

In figure 6 is shown the long preamble cross-correlator, which is designed by using a clipped long preamble cross-correlator [14].

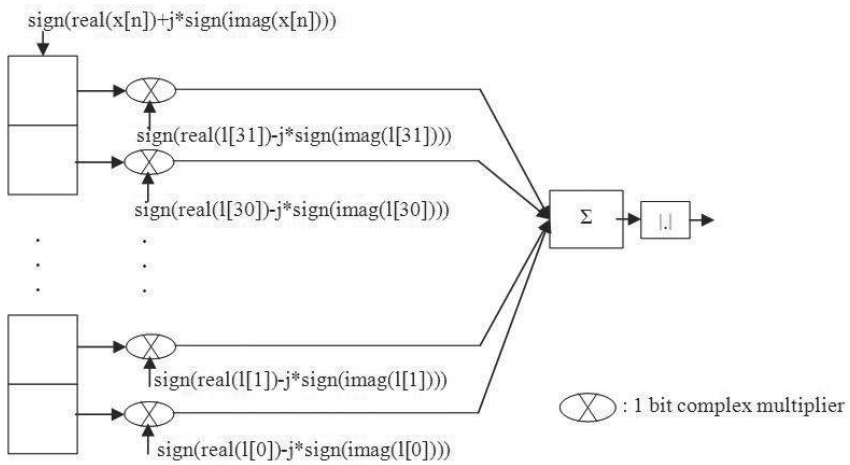


Figure 6 Long preamble correlator

Where, $x[n]$ is the incoming signal and $\{l[0], l[1], \ldots, l[31]\}$ is the long preamble sequence.

Channel equalization modules

The channel equalization modules perform a phase correction, an estimation of the channel transfer function and a channel cancellation. The phase correction circuit estimates the phase mismatch of pilot sub-carriers and performs linear interpolation. The phases of the 4 transmitted pilot sub-carriers are known and restricted to the set of values $\{0 , \pi\}$[2], then the estimated phase mismatch for the *n-th* pilot sub-carrier is $\arctan(\mathrm{Im}(H[k_{pn}])/\mathrm{Re}(H[k_{pn}]))$ or $\arctan(\mathrm{Im}(H[k_{pn}])/\mathrm{Re}(H[k_{pn}]))-\pi$; where, $H[k]$ is the COFDM symbol after timing synchronization and k_{pn} is the frequency bin of the *n-th* pilot sub-carrier. The phase correction of the 48 data sub-carriers is achieved by using linear interpolation, which is shown in figure 7.

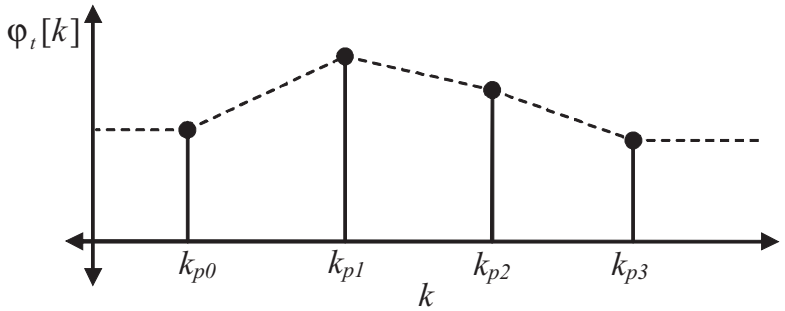


Figure 7 Phase linear interpolation

The dotted lines in figure 7 are the interpolated phases $\varphi_t[k]$ of the 48 data symbols after the FFT computation. The phase correction is accomplished by using the equation (4) .

$$H_c[k] = H[k]e^{-j\varphi_t[k]} \quad (4)$$

The phase correction circuit was designed by using a double-buffer, a polynomial estimator, a polynomial evaluator and Coordinate Rotation Digital Computer (CORDIC) [23] modules to evaluate the *atan(x)* and *exp(jx)* functions. Figure 8 shows the designed phase correction circuit; the polynomial estimator computes the slopes *m1*, *m2*, *m3* and the intercepts *b1*, *b2, b3* of the interpolation straight lines of $\varphi_t[k]$. The polynomial evaluator performs the interpolation by using the slopes and intercepts. The CORDIC modules compute the phases of the 4 pilot sub-carriers in vectoring mode, and the phase correction in rotation mode.

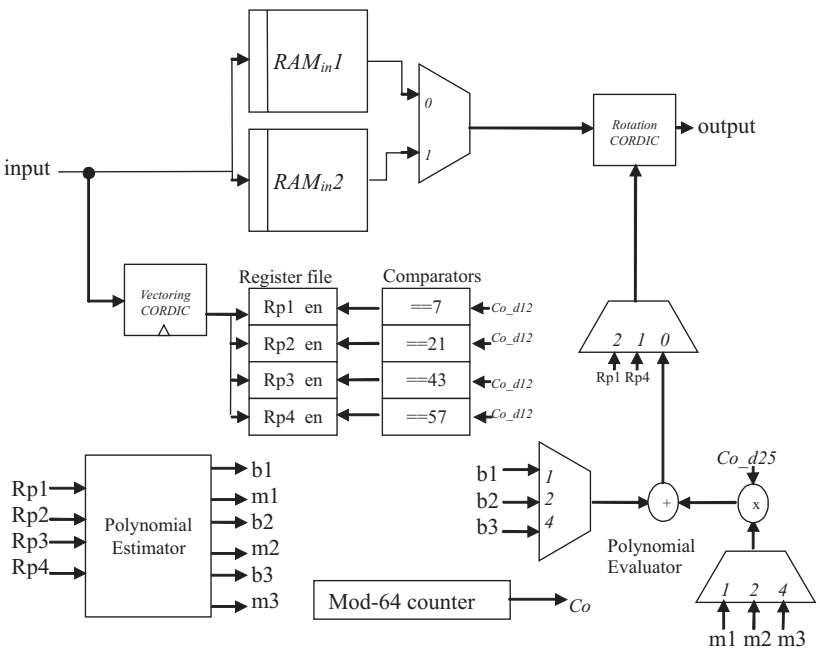


Figure 8 Phase correction circuit

The channel estimation is performed by computing $1/\hat{G}[k] = L_t[k] / L_r[k]$, where $1/\hat{G}[k]$ is the reciprocal transfer function of the channel, $L_r[k]$ is the DFT of received long preamble

sequence and $L_t[k]$ is the DFT of long preamble sequence. The channel cancellation is performed by computing $H_e[k] = H_c[k] / \hat{G}[k]$, where $H_e[k]$ is the equalized COFDM symbol.

The channel estimation-cancellation circuit shown in figure 9 was designed by using an SSRAM, a ROM, a complex multiplier and a complex divider.

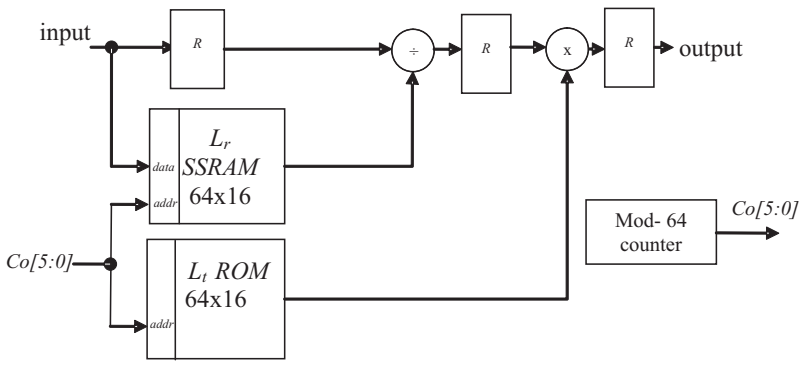


Figure 9 Channel estimation-cancellation circuit

The SSRAM stores $L_r[k]$ of each COFDM packet, and the ROM stores the pre-computed $L_t[k]$ used for all COFDM packets. The complex multiplier and the complex divider perform the channel cancellation for each received COFDM packet.

In-system hardware verification and results

Experimental setup

The COFDM baseband processor was tested by using the DSP Stratix II development kit [24], it uses the Altera FPGA EP2S60F1020C4. Table 1 summarizes the synthesis results of the designed COFDM baseband processor on the selected FPGA device.

Table 1 Synthesis Results of the COFDM baseband processor

Quantity/ Parameter	*Transmitter*	*Receiver*
Combinational ALUTs	1416	4060
Dedicated logic registers	1027	1699
Memory bits	26185	29294
Embedded multipliers	12	26
Maximum frequency (12/20 MHz clock domains)	291.04/109.03 MHz	55.65/137.27 MHz
Total Thermal Power Dissipation (two clock domains)	670.95 mW	705.60 mW
Total Thermal Power Dissipation (single clock domain 60 MHz)	728.66 mW	845.39 mW

The single clock domain COFDM baseband processor was synthesized adding two clock-enable signals activated each 5 and 3 clock cycles for the 12 Msymbols/s and 20 Msymbols/s blocks, respectively. Comparing the COFDM baseband processors, single and two clock domains, a power consumption reduction by 7,92 % is achieved in transmitter, and 16,54 % is achieved in receiver by using the two clock domains architecture.

To test the synchronization and equalization circuits, we implemented a RF sub-system operating at 2.4 GHz. The RF sub-system is composed of analog electronic circuits and a radiant system. The analog electronic circuits are: a RF mixer, a Voltage Controlled Oscillator (VCO) and a power amplifier. The radiant system consists of two monopole antennas for the transmitter and receiver. Figure 10 shows a block diagram of the RF sub-system, which is used in the transmitter and receiver into an indoor environment.

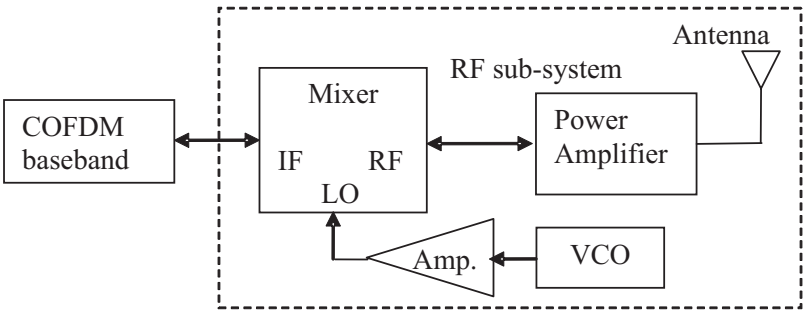


Figure 10 RF sub-system

The FPGA is connected to RF sub-system through the Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC) available on the development kit, this configuration is shown in figure 11.

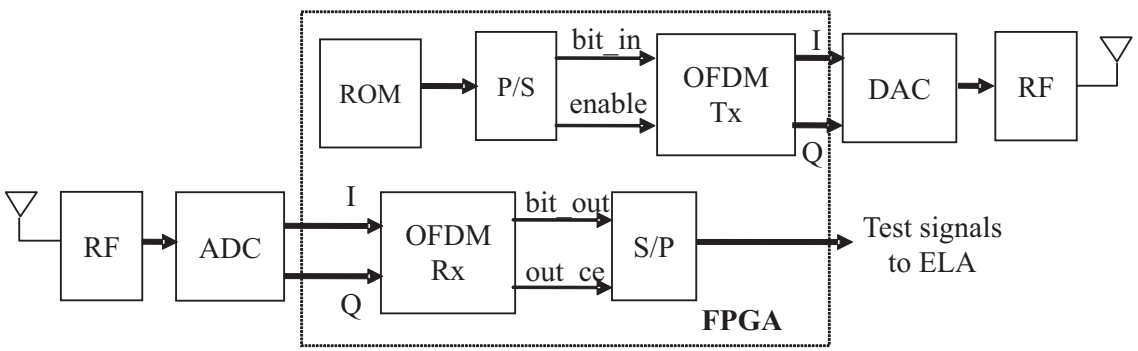
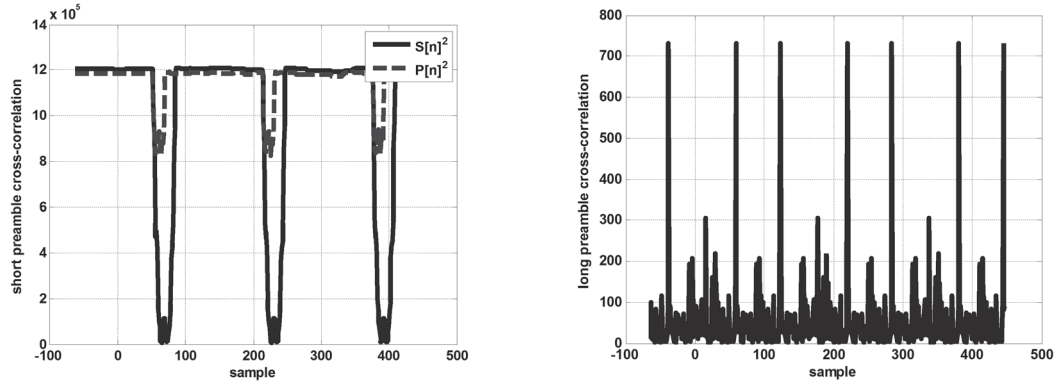


Figure 11 Setup for tests

Test signals were acquired in baseband frequency by using the Embedded Logic Analyzer (ELA) SignalTap II [25] and plotted by using MATLAB.

Test of timing synchronization circuits

The timing synchronization circuits are tested by using the short and long preamble sequences, which are generated in the COFDM transmitter and received by the short and long preamble correlators in the COFDM receiver. Figure 12(a) and (b) show the test results for the short and long preamble correlators, respectively.



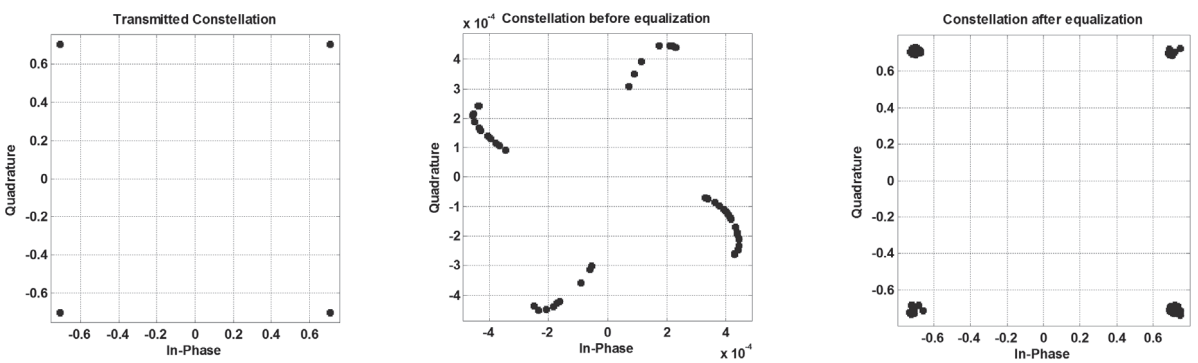
(a) (b)

Figure 12 (a) Short preamble auto-correlator test results, (b) Long preamble correlator test results

Figure 12(a) shows the signals $|S[n]|^2$ and $P^2[n]$ the short preamble auto-correlator. When $S^2[n_d] > tP^2[n_d]$, a new COFDM symbol is detected and this condition enables the long preamble correlator. Figure 12(b) shows the cross-correlation signal between received baseband signal and the long preamble sequence. When the cross-correlation signal reaches its maximum value, the COFDM data are detected after the cyclic prefix and demodulation system is enabled.

Test of channel equalization system

To test the channel equalization system the setup of figure 11 was used, where the ROM stores 256 random samples of 48 bits. The ELA SignalTap II acquired separately 256 sets of 48 QPSK symbols from mapper, FFT and channel equalizer; these symbols are acquired after the timing synchronization task is completed. Figure 13 shows three constellation plots for a single set of symbols generated in the transmitter, the receiver before channel equalization and the receiver after channel equalization.



(a) (b) (c)

Figure 13 Constellations during channel equalization process, (a) transmitted constellation, (b) constellation before equalization, (c) constellation after equalization

From figure 13(b) it can be seen that the QPSK symbols are rotated due to phase mismatch between local oscillator of transmitter and receiver, have reduced amplitude and are spread. Figure 13(c) shows the phase, amplitude, and spread correction of QPSK symbols.

Test of COFDM baseband processor

To test the COFDM baseband processor, the ROM in figure 11 stores a single-period sinusoidal wave of 256 samples of 12 bits each. Each sample was packed into a 48 bits frame; thus, a COFDM symbol represents a single sample of the sinusoidal wave. In this test, the frequency of transmitted sine wave is 12 MHz / 48 / 256 = 976.5625 Hz.

Figure 14 shows the acquired data with ELA SignalTap II.

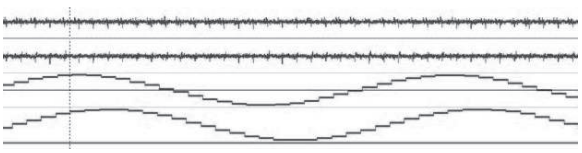


Figure 14 Test results of the COFDM baseband processor

The first two signals, upper side of figure 14, correspond to the transmitted COFDM symbol, which has a bandwidth of 20 MHz. The third signal is the transmitted sinusoidal wave and the fourth signal is the received sinusoidal wave. The COFDM baseband processor has a latency of 77 µs, which was measured by using the acquired data.

Conclusions

This paper presents the design and implementation of a full 12 Mb/s COFDM baseband processor that operates in the 2.4 GHz band and it is compatible with the IEEE 802.11a standard. This processor was designed by using two clock domains, which reduces power consumption by 7,92 % in transmitter and 16,54 % in receiver.

The designed processor includes our designed hardware circuits for synchronization and equalization; a short preamble correlator that uses smaller number of registers and multipliers than the ones reported in literature; a 12 Mbps Viterbi decoder based on double-buffer stages; and an improved R2^{2}SDF architecture for FFT.

Taking into account the obtained results, we can conclude that the designed COFDM baseband processor is suitable for implementing embedded wireless communication systems.

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