Electrical energy conversion system design with single-phase inverter and H5 transformerless topology

Diseño de un sistema de conversión de energía eléctrica con un inversor monofásico con topología H5 sin transformador

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Abstract

This paper presents the design of an electrical energy conversion system (EECS) for the use of solar energy and its conditioning for injection of energy to the commercial power grid. A single-phase full-bridge inverter with transformerless H5 topology coupled to an LCL filter is used. The system is identified using an averaged small-signal state space model; while the used cascade control scheme is tuned by pole placement and includes a maximum power disturb-observe tracking type algorithm of that increases efficiency by operating the system at the optimum operating point of the solar panel. This design describes essential technical aspects in the components sizing and selection for experimental development, as well as the control structure design for a good performance to face systems perturbations.

----------*Keywords*: single-phase inverter H5, solar energy, control systems, Unipolar PWM

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Resumen

Este artículo presenta el diseño de un sistema de conversión de energía eléctrica (SCEE) para el aprovechamiento de energía solar y luego acondicionamiento e inyección de energía a la red eléctrica comercial. Se utiliza un inversor puente completo monofásico con la topología sin transformador H5 acoplado a un filtro LCL. El sistema es identificado mediante el modelo de estado promediado y de pequeña señal, el esquema de control presenta un control en cascada sintonizado mediante la asignación de polos, además de un algoritmo de seguimiento de máxima potencia de tipo perturbar y observar que permite aumentar la eficiencia del sistema, operando en el punto óptimo de funcionamiento del panel solar. En el diseño se describen aspectos técnicos fundamentales en el dimensionamiento y selección de componentes para su desarrollo experimental, así como el diseño de la estructura de control para un buen desempeño ante perturbaciones del sistema.

----------*Palabras clave*: inversor monofásico H5, energía solar, sistema de control, modulación unipolar PWM

Introduction

Due to the high fossil fuels' costs and the various international agreements among industrialized countries to reduce CO_2 emissions, the use of renewable energy has increased in recent decades. In particular, systems for converting solar energy are considered the most viable alternatives amongst renewable energy technologies, which have been adopted throughout the world to meet the basic needs of electricity, particularly in difficult access remote areas [1]. For solar photovoltaic systems, the captured energy requires of electronic systems called power converters to adapt the initial current to the needs of its load [2]. Traditionally, this load is associated with AC through the commercial power grid, but can also be fitted for a DC bus in accordance with the new trends in micro and smart grid networks [3, 4]. In EECS from renewable sources, energy management is generally carried out by power converters. Efficiency and cost are important elements for selecting a particular topology. When inverters are connected to the network, it is common to use isolation transformers between the power converter and the grid. Often, these low frequency transformers are large in volume, weight and price, which make the converter unfeasible. In order to cope with this problem, a number of low power alternatives as transformerless topologies, have been suggested in the literature [5]. Using grid tied inverters without galvanic isolation between the solar panels and the grid can bring some major problems in their operation, as the common mode voltage and high leakage currents through the solar panels and installation. These problems may be caused by conditions such as humidity or even the way to setup [6]. The topology used in this work corresponds to the full-bridge or four switches H-bridge plus a fifth switch, hence the name H5. The technique developed by [7] is currently used by one of the largest worldwide inverters manufacturers as it is SMA. The topology is based on the full bridge and unipolar pulse-width modulation (PWM) technique. This technique allows a switched output current whose low frequency component is obtained by a third order LCL filter, which is dimensioned so as not posing a significant reduction in efficiency. This work proposes a cascade control structure that allows delivering electricity to the grid in compliance with known technical specifications and takes into account the increased use of energy supplied by solar panels.

Dimensioning of the power converter

The principle of operation of the H5 topology is based on the full-bridge inverter with a fifth switch that separates the solar panel power converter, as shown in figure 1. This topology is based on the use of the unipolar PWM modulation which allows, under the condition of zero voltage on the load of the unipolar modulation, opening the switch S5. The zero-voltage states are met when there is flow through switch S1 and the freewheeling diode of switch S3, or when there is circulation via switch S4 and diode of switch S2; both combinations only for the positive half cycle of the output current of the inverter. Similarly, for the negative half cycle combinations are: S2 when there is flow both in the S2 switch and the freewheeling diode of S4 or when there is circulation through switch S3 and diode of S1. If switch S5 is open, the generation stage is isolated from the converter and common mode voltages as well as leakage currents are reduced. Figure 2 shows the logical scheme of driving the switch S5 on the basis of the full bridge switches. A crucial aspect in the H5 topology is a suitable selection of S5 switch; as its performance can be affected by conduction losses of S5. This topology allows operating in two quadrants with a reduced number of components and a moderate yield. It also allows for a simple control structure with good performance against disturbances at the point of rated power. The full bridge inverter requires a configuration of anti-parallel diodes for each switch in order to allow conducting when inductive loads are presented. This case of study considers powers up to 1.5KW, so it is possible to use Mosfet transistors at 15 kHz switching frequency.
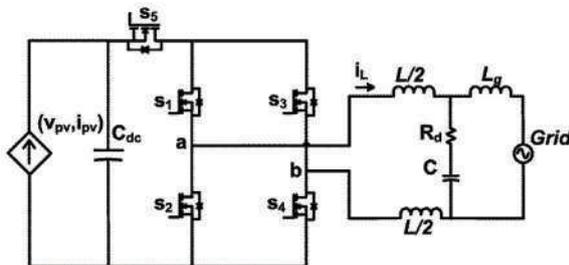
Figure 1 Full bridge inverter H5 and LCL filter scheme
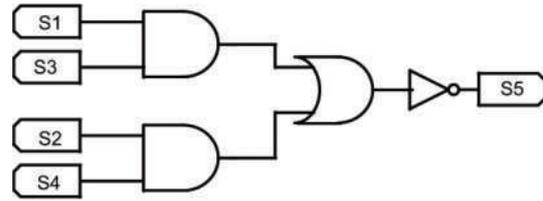
Figure 2 Logical switching scheme for switch S5

Solar panel model

One of the most important aspects in the design of the system shown in figure 1 is to specify the power and voltage of the solar array input panels. In this case, a set of 8 solar panels in series modeled with the features of SLK60P6L at 220W have been used. For maximum power, the equivalent solar panel can be modeled as shown in figure 3, where the point of maximum power output of the panel assembly is defined by $Ppv\_mppt = 1600W$ @ ($Vpv\_mppt = 200V$, $Ipv\_mppt = 8.07A$).
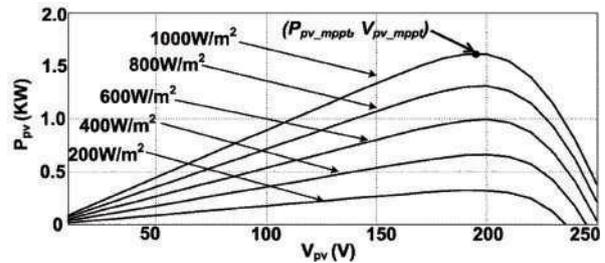
Figure 3 Equivalent power vs. voltage characteristic of the solar panel for different radiations @ T = 25 °C

Dimensioning the LCL filter

It is common to couple output filters to full-bridge inverter to reduce the high frequency components (harmonics) in the voltage and load current. In particular, in cases where low power converters inject power into the grid, it is necessary to comply with the standard for harmonic emissions IEC 61000-3-2, which applies to equipment connected to the grid with currents lower than 16A per phase. In this work the LCL filter type [8], with a dimensioning method that depends on the desired attenuation in the frequency

range, is used. Specifically, the LCL filter has an -60db/decade output current attenuation from its resonance frequency and thus low consumption of reactive power. The procedure for dimensioning the components of the LCL filter is presented in [8], where the current and impedance are determined based upon the nominal power value of $S_0 = 1500W$ and voltage $V_0 = 120V$, equations (1) and (2).

$$I_0 = \frac{S_o}{V_o} = 12.5\ A \tag{1}$$

$$Z_0 = \frac{V_o}{I_o} = 9.6\ \Omega \tag{2}$$

Once the system current and base impedance are known, the current consumption of the filter capacitor C is lowered to less than 5% of the rated current of the system to limit the power consumption, as shown in equation (3).

$$I_C = 0.05 \cdot I_o = 0.625\ A \tag{3}$$

Once known the capacitor current, the capacitive reactance and the capacitance C are determined by equations (4) and (5), at the network frequency $f_g = 60Hz$.

$$X_c = \frac{V_o}{I_C} = 192\ \Omega \tag{4}$$

$$C = \frac{1}{\omega_1 X_c} = 13.81\mu F, \text{con}\,\omega_1 = 2\,\pi\,fg \tag{5}$$

To calculate the inductor L, the criterion is to determine the maximum voltage drop across the inductor under nominal conditions. In this case, the inductive reactance X_L is fixed to less than 5% of the base impedance (equation 6), and the inductance L is calculated using equation (7).

$$X_L = 0.05 \cdot Z_o = 0.48\Omega \tag{6}$$

$$L = \frac{X_L}{\omega_1} = 192\ \Omega \tag{7}$$

For inductance L_g is necessary to define the resonance frequency. It is common to center it within the range defined in equation (8), which depends on the frequency of the network f_g and the switching frequency f_{sw} used by the converter.

$$10 \cdot f\_g < f\_resonance < /2\ \frac{f_{sw}}{2} \tag{8}$$

With this approach it is possible to reduce the switching harmonics located at twice the switching frequency and its multiples $(2 \cdot n \cdot f_{sw})$.

Equation (9) relates the resonant frequency of the filter and its components:

$$2 \cdot \pi \cdot f_{resonance} = \sqrt{\frac{L+L_g}{L \cdot L_g \cdot C}} \tag{9}$$

From equation (8), the resonance frequency $f_{resonance} = 4050Hz$ is fixed and through equation (9) the inductance $L_g = 0.11mH$. Another important factor in dimensioning the filter is the damping resistor R_d, which aids to limit the high gain of the filter at the resonant frequency. This damping resistor is calculated by studying its effect on the control loop, as presented later.

Dimensioning the capacitor "DC-link"

Within the required components in the system design, it is necessary to use a capacitor C_{dc}, commonly called "DC-link" capacitor which allows to significantly reduce the oscillations of the voltage at the inverter input and the variations around the operating point of the solar panel. A DC-link capacitor thereby contributes to increasing the system performance and performs well with stable dynamics in the control system. One of the criteria used for dimensioning the DC-link capacitor is to limit fluctuations to 5% of the voltage at the panel maximum power point $\Delta V_{pv\_mppt} = 0.05 \cdot V_{pv\_mppt}$. The relationship that limits ΔV_{pv_mppt} voltage variations as function of the rated power P_{pv_mppt}, f_g frequency network and capacitance C_{dc}, is given by equation (10), and yields $Cdc = 2.6mF$.

$$\Delta V_{pv\_mppt} = \frac{P_{pv\_mppt}}{2 \cdot f_g \cdot C_{dc} \cdot V_{pv\_mppt}} \quad (10)$$

Once the capacitance of the DC-Link capacitor is known, it is necessary to determine the maximum rms current at "rated power". This is because along with the operating temperature are the elements that significantly reduce its usage time [9]. Equation (11), used in [10], determines the current i_{c_dc} rms of the capacitor C_{dc} as function of the modulation index d, peak output current of the inverter $\hat{i}_L$ and phase angle between the voltage and current output φ.

$$i_{c\_dc} = \hat{i}_L \sqrt{\frac{d}{24\pi} \cdot [24 - 6\pi d + (8 - 3\pi d)\cos(2\varphi)]} \quad (11)$$

A rated power, the maximum current to circulate through the condenser C_{dc} is $i_{c\_dc} = 6.07A$.

Modeling and control system

Small signal model

In this part the dynamics of the power converter, the LCL filter and control system are studied. Firstly, the development of a small-signal model for the single-phase inverter is derived from a Buck converter [11] and starts from the average state model equation (12).

$$v_{ab} = (2d-1) \cdot v_{pv} \quad (12)$$

Where d is the amplitude modulation index, which relates the amplitude of the control signal and typical PWM modulation carrier signal [12]. From equation (12) a first order linearization is performed and set as criterion that variables expressed in lowercase, under the symbol "~", correspond to small-signal model variables and uppercase variables express the steady state operation. Thus, equation (13) expresses the equivalent model of the voltage in the power converter in steady state, while the small-signal model for the voltage and current is defined by equations (14) and (15) respectively. Figure

4 corresponds to the model of the considered circuit.

$$V_{ab} = (2D - 1) \cdot V_{pv} \quad (13)$$

$$\tilde{v}_{ab} = (2D - 1) \cdot \tilde{v}_{pv} + 2V_{pv} \cdot \tilde{d} \quad (14)$$

$$\tilde{i}_{pv} = (2D - 1) \cdot \tilde{i}_L + 2I_L \cdot \tilde{d} \quad (15)$$
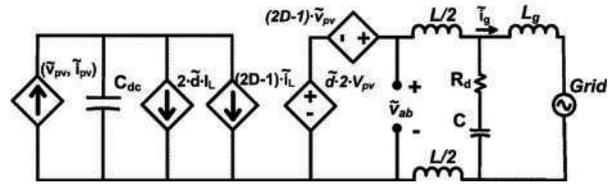
Figure 4 Small signal model for the power conversion system

From the small signal model shown in figure 4, the transfer function of the voltage versus modulation index is obtained in equation (16). Assuming that variations in the input voltage are negligible allows for a SISO type control system.

$$G_{i_{inv}}(s) = \frac{\tilde{v}_{ab}(s)}{\tilde{d}(s)} = 2 \cdot V_{pv} \quad (16)$$

Equation (17) shows the transfer function of the LCL filter used. This equation, together with equation (16) determines the overall transfer function of the process being controlled.

$$G_{f\_lcl} = \frac{\tilde{i}_L(s)}{\tilde{v}_{ab}(s)} = \frac{Z_{eq}}{sL_g \cdot (sL + Z_{eq})} \quad (17)$$

with $Z_{eq} = \frac{s^2 R_d C L_g + s L_g}{s^2 L_g C + s C R_d + 1}$

Figure 5 shows the frequency responses of the LCL filter for different values of R_d = [0, 3, 5, 10] Ω. It can be observed a significant increase in gain due to the resonance of the filter ($f_{resonance}$=4050Hz) when R_d=0Ω, which may cause serious problems in the performance of the control system. To solve this problem, it is proposed to incorporate the damping resistor R_d so significantly attenuates the gain at $f_{resonance}$. The

graph shows that as R_d increases, the filter gain does not vary significantly, but for frequencies near the resonance, it is attenuated completely. Importantly, as R_d increases the filter gain is reduced as well as the efficiency of the system.
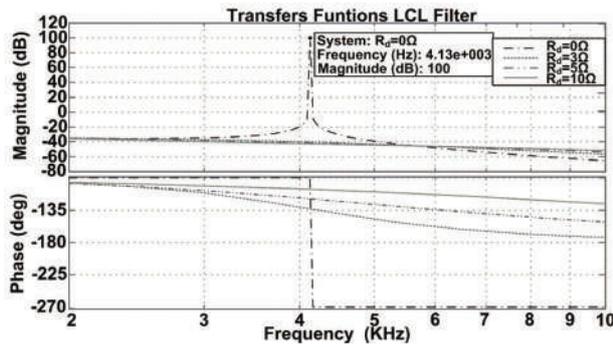
Figure 5 Bode diagram LCL filter

Current control loop

In relation to the control strategy, the average current control (ACC) technique is considered [13, 14], which allows using the average state model to half the switching frequency, so that the speed response of the control loops involved is connected with this condition. Once identified the control strategy is necessary to define the type of modulator. In this case, the unipolar modulation is used, which is a necessary condition for the H5 topology. This technique reduces the harmonic current injected to the network, especially in cases when the modulation index is low [15, 16]. Another advantage of the unipolar modulation technique consists in the considerable reduction of the rms current of the capacitor C_{cd}.

Equation (18) represents the transfer function of the modulator used in this application and corresponds to the double update PWM studied in [17], where the output signals to the comparator modulator are updated only when the carrier signal value reached minimum and maximum, as can be seen in figure 6.

$$G_{pwm}(s) = \frac{1}{2 \cdot V_{pp}} \left(e^{-s(1-D)T_s} + e^{-sDT_s} \right) \quad (18)$$
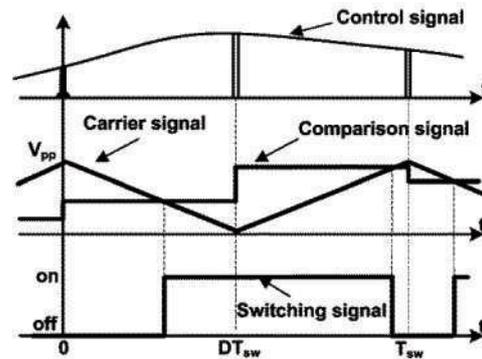
Figure 6 Double update PWM Modulator

This transfer function is dependent on the peak to peak amplitude of the triangular comparison signal $V_{pp}=1$ of the duty cycle D, which in this case is considered as an average value of a switching cycle (D = 0.5), and the maximum time delay expressed as $T_s=0.5T_{sw}$.

In order to facilitate the study of the control loops in continuous time, and in turn introduce the effects of the delay resulting from the digital sampling into the temporal analysis, the second order Pade approximation given in (19) [18] has been used in the transfer function (18).

$$e^{-sT_s} \approx \frac{1-0.5T_s \cdot s+0.083 \cdot (T_s \cdot s)^2}{1+0.5T_s \cdot s+0.083 \cdot (T_s \cdot s)^2} \quad (19)$$

Figure 7 illustrates the block diagram of the proposed control system after modeling the elements of the energy conversion system. This diagram has a cascade control, where the inner loop controls the output current of the LCL filter in terms of the modulation index amplitude d. The outer control loop is used to regulate the voltage of the panel. This control variable is important because it is closely related to the maximum power point of the solar panel. The voltage control loop is responsible for setting the amplitude of the reference current and with the PLL synchronization algorithm provides a sinusoidal reference current in phase with the network voltage V_{red}. This algorithm is used in [19] and is not part of interest of this work. It is worth mentioning that within the control system also operates a maximum power search

algorithm, responsible for setting the reference voltage V_{pv_ref} for voltage control loop, which will be discussed later.
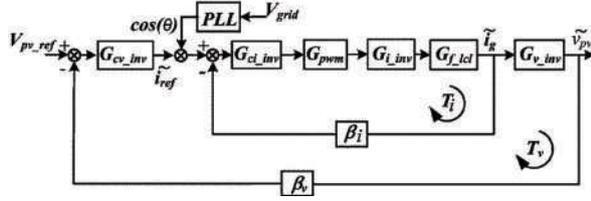
Figure 7 Voltage and current control loop

For the stability analysis of the current control loop, the open loop gain shown in equation (20) is used.

$$T_i = G_{ci\_inv} \cdot G_{pwm} \cdot G_{i\_inv} \cdot G_{f\_lcl} \cdot \beta_i \qquad (20)$$

Where β_i is the gain of the current sensor, which in this application $\beta_i=1$.

Regarding the G_{ci_inv} function, which corresponds to the controller, the proportional plus resonant type formulated in (21) has been selected, which allows tracking the reference current in addition to introducing a control loop gain at the network frequency that improves the distortion of the injected current for frequencies near f_g. For tuning the controller parameters, the value of k_p was selected using pole placement technique. This technique allows to determine the controller gain k_p such that bode diagram of the open-loop gain T_i exhibits a very similar dynamics to a pure integrator "1/s", with a gain margin GM > 6db and a phase margin MF > 50 °, if the zero crossing frequency is lower than half of the switching frequency (frequency where the average states model becomes invalid). A value of $k_p = 0.05$ is obtained by applying the methodology described above.

$$G_{ci\_inv} = k_p + \frac{k_h \cdot B_h \cdot s}{s^2 + B_h \cdot s + \omega_h^2} \qquad (21)$$

In relation to the resonant control parameters, these have been tuned as follows: $k_h=5$ is the gain of the resonant peak, $B_h=4\cdot\pi$ rad/s is the bandwidth of the resonant peak and $\omega_h=2\cdot\pi\cdot60$

rad/s determines the frequency of the desired resonant gain [20]. Figure 8 illustrates the behavior of the current control loop where the frequency response is observed. In the case when $R_d=0\Omega$, the loop gain at the resonance frequency is high, jeopardizing the stability of the system, reason why the inclusion of the damping resistor $R_d=3\Omega$ and the proportional control is suggested. With this control the frequency response is stable. The contribution of the resonant control ensures that the output current present less distortion, the proposed controller has a PM= 56.6 °, a GM=11db and a zero crossing frequency $f_{Ti\_crossing}=637Hz$, so the system stability is guaranteed.
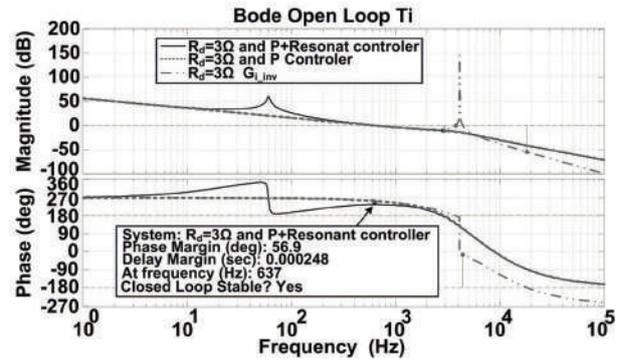
Figure 8 Frequency response of the current loop T_i

Voltage control loop

Once the response speed of the current control loop for zero crossing frequency is set, the voltage transfer function is determined using equation (22). This function is valid assuming $\tilde{i}_{ref} \approx \tilde{i}_g$ for frequencies below the zero crossover frequency of the loop current control.

$$G_{v\_inv} \approx \frac{-1}{C_{dc}\cdot s} \qquad (22)$$

The loop gain for the voltage regulation v_{pv} is given by equation (23), where it was considered that the gain of the sensor voltage is $\beta_v=1$.

$$T_v = G_{cv\_inv} \cdot G_{v_{inv}} \cdot \beta_v \qquad (23)$$

Given its characteristic, the transfer function for $G_{v\ inv}$ corresponds to PI controller shown in equation (24).

$$G_{cv\_inv} = K_{pv} + \frac{k_i}{s} \qquad (24)$$

The voltage controller tuning is performed, as in the current control by pole assignment at zero crossover frequency near 63.7Hz. This frequency is located a decade below to the response of the current loop, although this frequency might include dynamics affecting the harmonic distortion in the current reference of the inner loop, so it is suggested to decrease it according to the commitment efficiency vs. harmonic distortion permitted by the system. With these assumptions, the values of K_{pv} and K_i are obtained as 0.4 and 24, respectively. The frequency response of the voltage control loop is depicted in figure 9, showing a stable behavior with an MG = 36db and an MF = 79.6°.
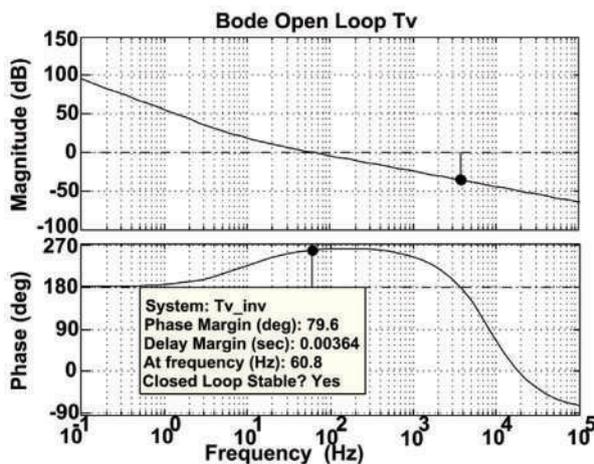
Figure 9 Frequency response of the voltage loop T_v

Tracking maximum power point algorithm (MPPT)

Since the maximum efficiency point of the solar panel varies depending on the solar radiation and has non-linear dynamic behavior, it is necessary to use a maximum power tracking algorithm. There are several types of this technique, but due to its simplicity, perturb & observe technique P&O [21] is one of the most widely used, because it is not necessary to know the model of the energy conversion system. In this case, the algorithm defines the reference voltage V_{pv_ref} shown in figure 7. For tuning the algorithm a stabilization time t_s=25ms and step size ΔV_{ref}=1V are used.

Performance of the power conversion system

Once the solar energy conversion system using the parameters shown in table 1 and the power electronic circuits *Psim® 7.0* simulation software is designed, it is possible to observe the behavior of the system to a disturbance in the solar incidence with 200W/m² steps, starting in 200W/m² and ending at 1000W/m². Figure 10 includes the behavior of the current loop in the inverter. It is possible to observe the increase of the current delivered to the network in proportion to the increase in solar radiation incidence. Likewise is noted that the current regulator allows the current to follow the reference controlled with stable dynamics.

Table 1 Specifications design and circuit parameters

Description	Value
P_{pv-max}	1600 *W.*
f_{sw}	15*kHz*
f_g	60*Hz*
L	5.26*mH*
L_g	0.11*mH*
R_d	3Ω
C	13.81µF
C_{dc}	2.6*mF*
V_o	120*V rms*
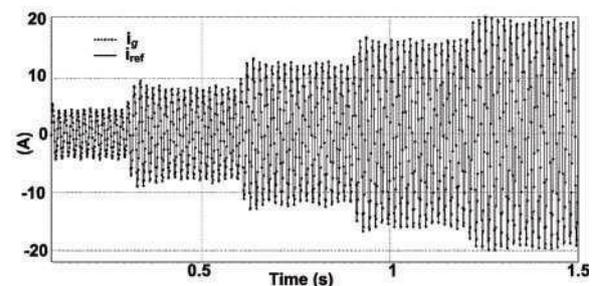
Figure 10 Output current behavior I_g to different solar radiation steps

Figure 11a is an enlargement of figure 10, which shows that for a solar irradiation of 200W/m² an output current with an amplitude of I_g=2.9A rms and distortion near THDi<5% is obtained. Figure 11b illustrates the behavior of the output current at nominal power. If solar irradiation were 1000W/m², would have an amplitude of I_g=13.5A rms and THDi<2%, enabling compliance with the IEC 61000-3-2 standard, which relates the harmonic distortion to equipment connected to the network.

Figure 12 shows the voltage loop behavior which chatters around the reference voltage set by the MPPT algorithm. Ripple is closed to the fixed by capacitor C_{dc}. The same figure shows that the output current I_{pv} of the solar panel increases proportionally to the power P_{pv} handled by the system.
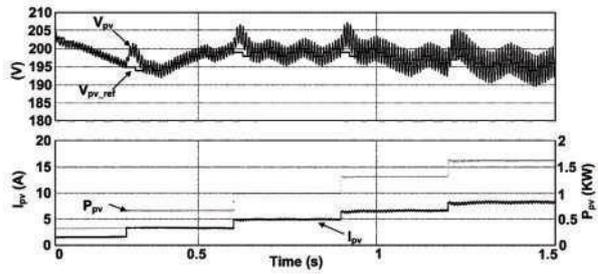
Figure 12 Behavior of the control loop voltage and MPPT algorithm

Figure 13 shows the performance of the maximum power tracking algorithm MPPT. Due to its oscillating nature, this algorithm operates around the maximum power point for each case of solar irradiation.
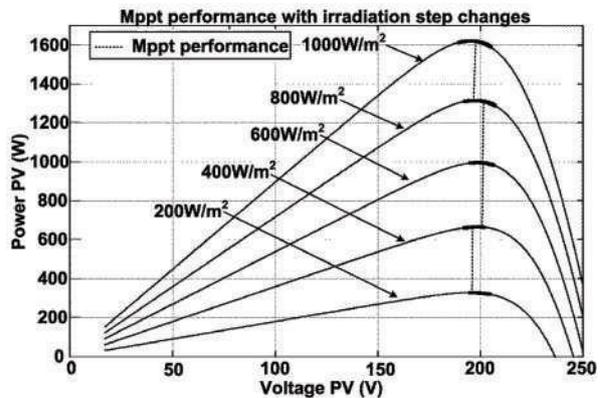
Figure 13 Performance of the maximum power tracking algorithm MPPT

a)

b)

Figure 11 Enlargement of figure 10. Output current I_g

Conclusions

This paper has considered a solar energy conversion system that consists of a full-bridge inverter with transformerless H5 topology

coupled to a LCL filter. The advantage of this topology is to reduce common mode currents isolating the inverter from the solar panel by means of an additional switch instead of the classic full-bridge inverter. The control scheme contains a cascade control and a maximum power tracking algorithm operating near the maximum performance point, which allows power delivery to the grid with low distortion. The presented design is a viable solution for low power applications, since it is possible to remove isolation by low frequency transformers, which in most cases increases the cost and size of inverters. Dynamic performance under varying solar incidence has been stable and the results have been verified by computer simulation with the simulation software *Psim*® 7.0

Acknowledgments

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